Study of a solar cell with a silicon-based photodiode structure

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Abstract. This article presents the results of a study of the capacitance-voltage characteristics of MSM photodiode structures with silicon-based potential barriers. The results of studies aimed at creating Au-nCdS-nSi-pCdTe-Au photodiode structures for the spectral range of 1.0-1.4 microns with an area of 29 mm^2, which were obtained by vacuum evaporation in a quasi-closed volume of sputtering layers of cadmium sulfide and cadmium telluride, are presented. onto a silicon substrate with resistivity ρ = 607.47 Ohm·cm. A distinctive feature of the resulting photodiode Au - nCdS-nSi - pCdTe - Au structures are two-way sensitive and have a low capacitance value of C = 23.3 pF at room temperature.

1 Introduction

Optical systems for transmitting and receiving information, being an alternative to cable transmission, are beginning to become widely used [1-5]. Their important elements are receiving optical modules, the functions of which include converting the optical signal received by the photodetector into an electrical one, which is processed by electronic devices. At the same time, the photodetector is required to capture even a very weak optical signal, low inertia and noise [6-7]. Phototransistors and photodiodes without charge accumulation meet these requirements to a certain extent. However, the time constant of a phototransistor is longer than that of a photodiode, which limits its application in communication systems [8]. The above problem can be solved by creating structures with two Schottky barriers based on silicon. The appeal to silicon is due to the fact that it is the most technologically proven, well-developed material, however, photodiode strucures with two barriers and based on it remain poorly studied. In a photodiode structure, the creation of a second or third barrier helps to reduce its capacitance [9], enhance the primary photocurrent [10], and increase the frequency range and speed of operation [11].

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2 Experimental samples and research methods

The heterojunction photodiode structure Au - nCdS-nSi - pCdTe - Au was obtained in a quasi-closed volume by vacuum thermal evaporation of CdS and CdTe powders onto a single-crystalline n -type silicon substrate with film thickness d = 0.55 μm, determined with an MII-4 microinterferometer.

The substrate is single-crystal n -type silicon of the KEF-600 brand according to TU 48-4-295-82 with a thickness d = 130 μm and a diameter D = 42 mm with a resistivity of 607.47 Ohm·cm, oriented in the crystallographic direction (111) and concentration of the main carrier's component Nn = $7\cdot10^{12}$ cm^{-3}.

Using the method of vacuum evaporation in a quasi-closed volume [11] makes it possible to obtain layers with thicknesses ranging from several hundred angstroms to several tens of microns. At the same time, homogeneity and maximum frequency of the material are achieved, and film growth conditions are easily controlled.

N-type CdS powder with a particle size of 120 μm and a purity of 99.99 % was used as the starting material to obtain the Au-nCdS-nSi-pCdTe-Au photodiode structure. 60 μm p-type CdTe with 99.999% purity from Advanced materials (China). The resistivity of CdTe is $\rho \approx 10^4 \div 10^6$ Ohm·cm, and the resistivity of CdS $\rho \approx 10^2$ Ohm·cm. The concentration of the main carriers of CdTe is $N \approx 10^{12} \div 10^{14}$ cm^{-3}, CdS = 10^{18} cm^{-3} [12-13]. CdS and CdTe films were deposited by vacuum evaporation on the silicon surface of an AVP-05 unit, at a pressure in the chamber P = $1.8\cdot10^{-5}$ mm Hg. The installation diagram of the AVP 05 vacuum unit is shown in Fig. 1.

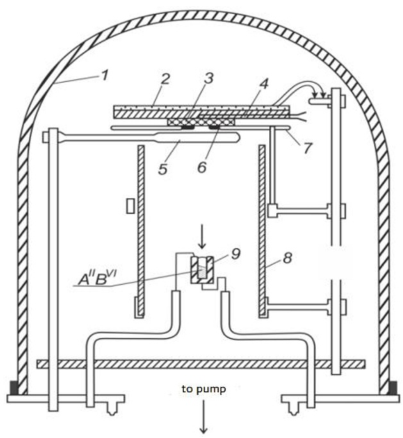


Fig.1. Diagram of a vacuum chamber for film deposition using thermal evaporation in a vacuum: vacuum unit - AVP 05 glass cap; 2 - substrate heater; 3 - substrate; 4 - thermocouple; 5 - movable damper; 6 - mask; 7 - mask holder; 8 - internal reflector; 9 - evaporator.

When depositing CdS films on the surface of a silicon substrate, the evaporator temperature was varied in the range Ti = 750÷800°C, necessary for congruent evaporation of CdS particles, in which the temperature of the silicon substrate was simultaneously maintained in the range Ti = 200÷250°C. At a low temperature of the silicon substrate, fine-grained and randomly oriented grains are formed in the polycrystalline film. CdTe films were deposited on the back side of the substrate at an evaporator temperature Ti = 550 °C.

During the deposition of CdTe films, the substrate temperature was TS =270÷290 °C. The film growth time is t = 5 minutes at a rate of υ = 16.7 Å/s, at which the thickness of each film is 0.55 μm. The thickness of the films was measured with a Linnik MPI-4 microinterferometer. The data obtained when studying the surface using a MII-4 microscope showed that a thin layer of CdS deposited on the surface of the n Si substrate consists of columnar crystallites, misoriented in azimuth and oriented in the direction of film growth [14].

To obtain a rectifying contact on the surface of the film layers of the heterostructure, metal-semiconductor transitions obtained by sputtering gold (Au) with a thickness d = 100 Å in a VUP-4 vacuum station at a temperature T = 435 ° C. Next, the resulting heterojunction structure Au - nCdS-nSi - pCdTe - Au scribed into discrete samples with an area of 29 mm^2.

The capacitance-voltage characteristics of the studied heterostructures were measured with a capacitance value in the range C = 0.1÷50 nF on a standard installation, according to the block diagram shown in Fig. 2. From a source of stabilized constant voltage through a variable resistor R with a nominal value of 5000 Ohms and through a constant resistance Rs, voltage was supplied to the sample being measured through the probe. The value of Rs was chosen based on the minimal influence of the installation capacitance on the measurement error.

From the measuring probe, through the decoupling resistor R in 1, the voltage was supplied to the DC millivoltmeter Shch-300, operating in the mode of measuring the bias voltage, supplied to the structure under study and through the DC decoupling capacitance C pp. From the capacitance C pp 0, the signal was supplied to the automatic AC bridge Shch-5048, operating in capacitance measurement mode.

Capacity Cpp and Cx form one of the arms of the automatic compensation method of measurement using the Shch-5048 device. The device takes measurements at three fixed capacitance measurement frequencies, F =50 Hz, 1000 Hz and 10000 Hz and displays the result on a six-digit digital indicator. The speed of the bridge (number of measurements per second) is set smoothly using a regulator.

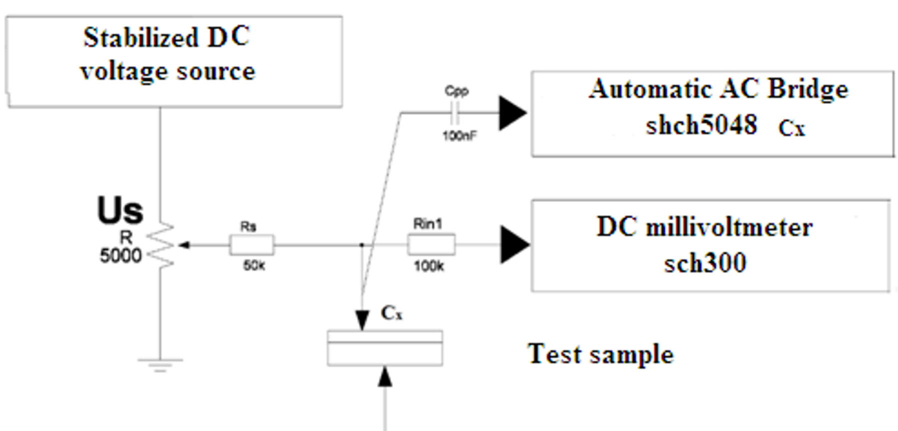


Fig.2. Block diagram of measuring the capacitance-voltage characteristics of a double heterostructure Au - nCdS - nSi - pCdTe - Au.

Light current-voltage characteristics of photosensitive Au-CdS-nSi-CdTe-Au heterofilm structures were measured in the forward and reverse directions of current. The current-voltage characteristics were taken at room temperature T = 20ºC with illumination E = 0÷160 lux. The structures were illuminated from a special incandescent lamp SIRSH 6-100 with a power of W = 100 W, which in its parameters is identical to the standard white light lamp. It should be noted that one lumen of electromagnetic radiation in the visible region of the spectrum contains a power of 9.1·10-3 W.

3 Results and discussion

Voltage-capacitance characteristics (VCC) of the heterostructures under study Au - nCdS - nSi - pCdTe - Au were measured with a capacitance value in the range (0.1÷50 nF) at room temperature 25 ºC in forward and reverse switching modes in the frequency range *f* = 0.4÷50 kHz. VEHs at these frequencies have the same shapes (Fig. 3). When measuring capacitance, the choice of frequency depends on the capacitance of the structure.

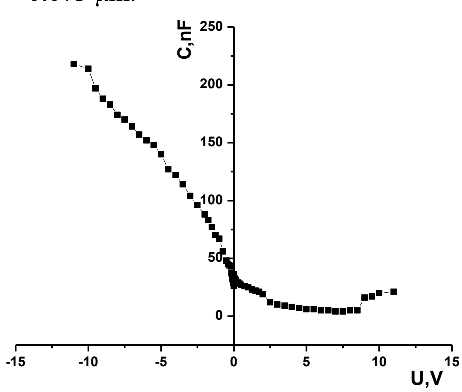
When sputtering films of the nCdS and pCdTe types onto the silicon surface, they manifest themselves as high-resistivity, *i* -layer makes it possible to form transition *i -layers of* the nCdS-nSi and pCdTenSi interfaces on the boundary layer.

Based on the capacitance of flat zones and the steep section of VCC, the concentration of equilibrium electrons is determined - n_0. To determine n_0 according to the VCC characteristic, a curved section with two slopes was built in C^{-2} (U) coordinates: section 1 and 2 (Fig. 1). According to the well-known formula (1) [10].

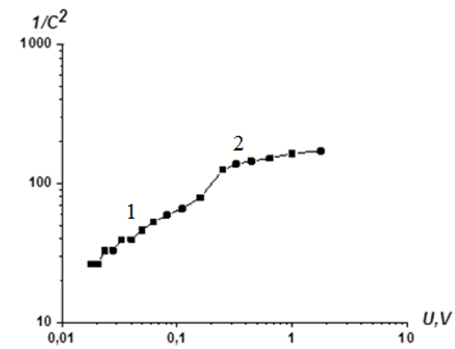
$$n_0 = \frac{2}{q\varepsilon_0\varepsilon_S S^2}\frac{dV_D}{d(C^{-2})}, \quad (1)$$

the concentration of equilibrium electron carriers was determined.

By capacity C_i = 217 nF using the formula of a flat capacitor, the thickness d_i is determined = 0.011 µm. Based on the minimum structure capacitance C_{min} ≈23.3 nF, the space charge thickness W ≈ 0.103 µm was determined. At thermodynamic equilibrium, its thickness, which was calculated from a capacitance of 31.7 nF in the absence of bias voltage, is ~ 0.073 µm.



Dependence of C(U) for forward and reverse voltage bias



Dependence C^{-2}(U) for a typical sample of heterostructure

Fig. 3. Voltage-capacitance characteristics of Au - nCdS - nSi - pCdTe - Au heterostructures at frequency *f* = 10 kHz and T = 25 ºC

The concentration of equilibrium electron carriers is $N_C \approx 3.3\cdot10^{15}$ cm^{-3} and $N_V \approx 4.1\cdot10^{14}$ cm^{-3}. By extrapolating the C^{-2} (U) dependence onto the voltage axis U (Fig. 1) with the value of the structure capacitance C = 24 nF, V_D was determined = (0.843 ± 0.02) eV for n_0 in nSi . In addition, the value of the concentration of equilibrium electrons was estimated from the capacitance of flat bands [15]. The value of n_0 determined by VCC is combined with the value of the equilibrium electron concentration of $3.6\cdot10^{12}$ cm^{-3} for n-Si.

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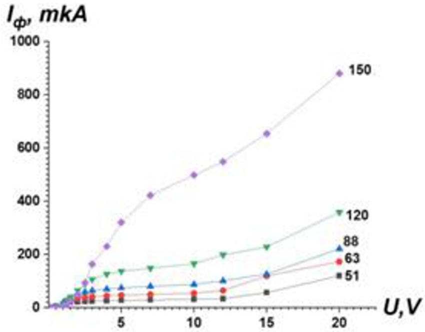
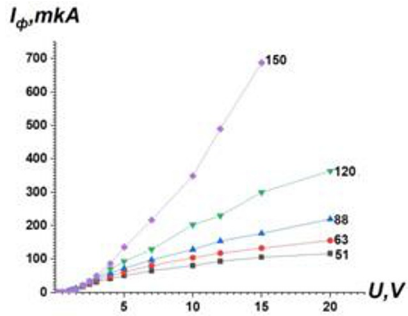


In forward bias mode



In reverse bias mode

Fig. 4. Dependence of photocurrent on operating voltage when excitation of transitions of the Au-CdS-nSi-CdTe-Au structure sides with integral light at different illumination intensities (Lux) of the CdTe-Au junction

Dark and light current-voltage characteristics of photosensitive heterofilm Au-CdS-nSi-CdTe-Au structures in the forward and reverse directions of current were photographed at room temperature 20ºC, the illumination of the structure was within the range E = 0÷160 lux. At different light intensities integral source with a maximum at λ=0.55 µm, illuminating the surfaces of both sides of the photosensitive Au-CdS-nSi-CdTe-Au structure, i.e. when excited by light with an energy greater than the band gap of the base region, they showed that as the illumination intensity increases, the dependence of the photocurrent on the operating voltage becomes linear and sublinear in nature, with reverse and forward voltage biases (Fig. 4 and 5).

As follows from measurements of the lux-ampere characteristics of Au-nCdS-nSi-pCdTe-Au structures (Figs. 4 and 5), almost all curves have several inflection points with subsequent saturation. These points are located approximately in the same range of power values incident on the structure.

Absorption of radiation in the near-surface region of the semiconductor, as well as separation of carriers by the barrier field formed at the interface of the nSi - p CdTe or n CdS-nSi contact, causes kinks in the region of low input power levels (0÷90 lux). These kinks are due to the fact that more powerful radiation (100÷160 lux) is absorbed by deeper layers of the heterostructure.

Charge carriers generated by radiation of this level of power are separated by the field of the nSi - p CdTe and n CdS-nSi heterojunction. A similar jump in the photocurrent in the region of low levels of input power is due to the separation of carriers by the *p* - n field and n - *p* junction existing in a multilayer heterostructure Au - n CdS-nSi - p CdTe-Au.

Based on the analysis of the inverse current-voltage characteristic, it was revealed that thermionic currents flow in the structure at current density range $I \approx (1.3 \cdot 10^{-9} \div 1.1 \cdot 10^{-8}$ A/cm^2) and photosensitivity value $S_\lambda = 2.02 \cdot 10^{-4}$ A /W. The flowing thermionic current is described using formula (2): [16]

$$\boldsymbol{J} = \boldsymbol{J_{01}}\, \boldsymbol{exp}\left(\frac{\mathrm{eV}}{\boldsymbol{C_1 KT}}\right) + \boldsymbol{J_2}\, \boldsymbol{exp}\left(\frac{\boldsymbol{eV}}{\boldsymbol{C_2 KT}}\right) \qquad (2)$$

The values of the pre-exponential factor "J_0" and the exponent "C" are given in Table 1.

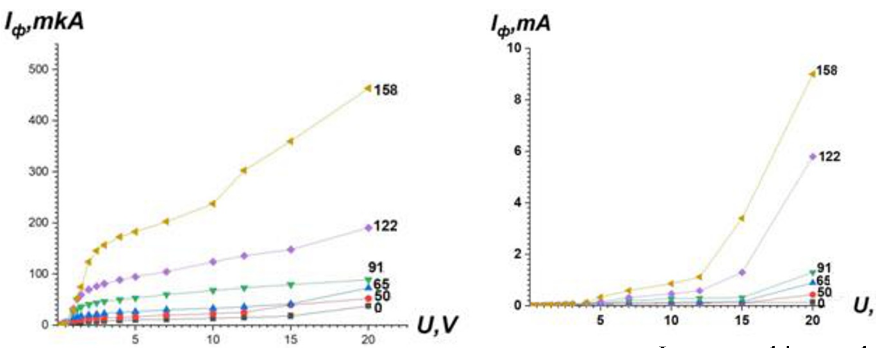
Table 1.

Values of the pre-exponential current multiplier "J_0" and the exponent "C" of the photosensitive Au-nCdS-nSi-pCdTe - Au structure

Table 1. The pre-exponential factor

Illuminated layers in the structure Au - nCdS - nSi - pCdTe - Au	Pre-exponential current multiplier	Exponent exponent	Pre-exponential current multiplier	Exponent exponent
	J_{01}, A	C_1	J_{02}, A	C_2
Au - nCdS	$4.5 \cdot 10^{-7}$	2.3	$5.3 \cdot 10^{-8}$	1.3
Au - pCdTe	$6.7 \cdot 10^{-6}$	3.7	$3.2 \cdot 10^{-9}$	1.5

The above estimates of the pre-exponential factor show that in Au-CdS-nSi-CdTe-Au structures at low illumination levels, the current is mainly limited by recombination in the space charge layer, and at high illumination levels, diffusion currents of non-major nonequilibrium photocarriers begin to contribute to the photocurrent.



In forward bias mode In reverse bias mode

Fig.5. Dependence of the photocurrent on the operating voltage when excitation of the transitions of the sides of the Au-CdS-nSi-CdTe-Au structure with integral light at different illumination intensities (Lux) of the Au - n CdS junction

In practice, it is very important to obtain the maximum power per unit area of the photodiode. In these structures, the accumulation of current carriers moving to the upper heavily doped wide-gap semiconductor n CdS-nSi also plays a decisive role. the generated electron-hole pairs are separated by the electric field of the space charge at these structure boundaries.

Holes freely drift along the field deep into the semiconductor, and electrons on their way encounter a barrier at the boundary of nSi - p CdTe and n CdS-nSi, which is a transition i-layer and accumulate in the potential well and, therefore, increases the likelihood of tunneling through the transition i-layer. In a stationary state, an equilibrium is established between the flows of electrons leaving the illuminated layer and entering the well due to photogeneration. Assuming that the main mechanism of photocurrent is the accumulation of of the majority carriers and their tunneling through the barrier created by the boundary i-layer, one can estimate the maximum permeability of the barrier, with a non-decreasing photocurrent.

In Fig.6 the direct (*I*) and reverse (*II*) branches of the current-voltage characteristics (CV characteristics) of the heterojunction are presented Au - nCdS-nSi - pCdTe - Ag structures, which were measured at room temperature and plotted on a log-log scale.

The direct branch of the current-voltage characteristics of Au - nCdS-nSi - pCdTe - Au structures is well described by power-law dependences of the type - $I = AV^{\alpha}$ with different values of the exponent α. Analysis of the direct branch of the current-voltage characteristic shows that at room temperature there are three pronounced sections in the voltage range from zero to 3 V - $J \propto V^{2.44}$ (1), in the range from 5 to 40 V - $J \propto V^{0.78}$ (2) , in the range from 43 to 50 V - $J \propto V^{5.55}$ (3).

According to theory [8], diode structures have a power-law dependence of current on voltage of the type $J \propto V^{\alpha}$, ($\alpha \geq 2$), including a region of sharp increase in current when complex defect-impurity complexes are involved in recombination processes along with point defects, within which electron exchange occurs [9] .

$$U = N_R \frac{c_n c_p (pn - n_i^2)}{c_n(n+n_1) + c_p(p+p_1) + a\tau_i pn}, \quad (1)$$

where N_R is the concentration of recombination centers (complexes), n, p are the concentrations of electrons and holes, n_i is the intrinsic concentration in the semiconductor, c_n, c_p are the capture coefficients of electrons and holes, n_1, p_1 are the equilibrium electron concentrations and holes in conditions

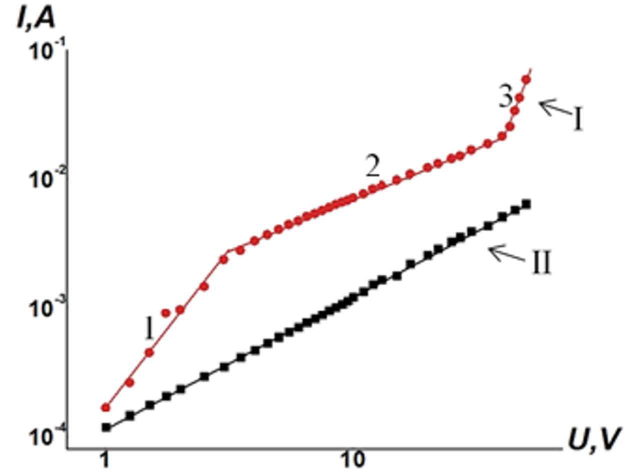


Fig. 6. Current-voltage characteristic Au-nCdS-nSi-pCdTe-Au heterostructures in the voltage range from zero to 3 V - $J \propto V^{2.44}$ (1), in the range from 5 to 40 V - $J \propto V^{0.78}$ (2), in the range from 43 to 50 V - $J \propto V^{5.55}$ (3).

when the Fermi level coincides with the impurity level (the so-called Shockley -Reed static factors), τ_i is the time that takes into account certain electron exchange processes within the recombination complex, *a* is a coefficient depending on the specific type of impurity or defect-impurity complexes.

The nCdS-nSi - pCdTe structure under study may contain point defects - vacancies of both cadmium (Cd) atoms and sulfur (S) or tellurium (Te) atoms.

In the sub lattice of cadmium atoms, singly and doubly charged vacancies $\mathbf{V_{Cd}^{-}}$, $\mathbf{V_{Cd}^{2-}}$ are easily formed. Doubly charged vacancies of cadmium atoms in most cases form complexes with positively charged impurities of the type $(\mathbf{V_{Cd}^{2-}}\ D^{+})^{-1}$ and neutral sulfur atoms of the type $(\mathbf{V_{Cd}^{2-}}\ S^{*})^{-2}$. In addition to these complexes, there is a high probability of the formation of such defect-impurity complexes, such as “negatively charged acceptor + positively charged interstitial ion” or “positively charged donor + negatively charged vacancy” [17], which play a decisive role in recombination processes.

Based on the data calculated from the experimental results, a band diagram was constructed
Au-nCdS-nSi - p CdTe-Au heterostructure, which is shown in Fig.7. From the band diagram of the heterostructure it is clear that forward and reverse currents are limited by the resistance of the space charge layer at the interface of the nCdS - n Si and n Si-pCdTe heterojunction. This space charge consists of negatively charged mobile and immobile donor centers, which are located in the nCdS and - p CdTe layer adjacent to silicon, respectively, since the donor concentration in nSi is ten orders of magnitude greater than the carrier concentration in these layers.

In this structure, the contact between Si and nCdS also gives a contact potential difference of U = 1.1 eV, however, an enriched layer of space charge appears at the interface of the Si and nCdS layer, since the work function of the metal (Au) present in large quantities in *n* CdS layer is less than the work function of the semiconductor - Si.

When illuminated from Au - n CdS-nSi - p CdTe-Au heterojunctions from the rear sides, photogeneration of film carriers of chalcogenide compounds nCdT e and pCdS occurs. The main current carriers diffuse into the n -layer of silicon, where they are separated by the transition field with further acceleration of the carriers by the applied external field, sufficient for impact ionization of Si atoms, which leads to the development of the avalanche process.

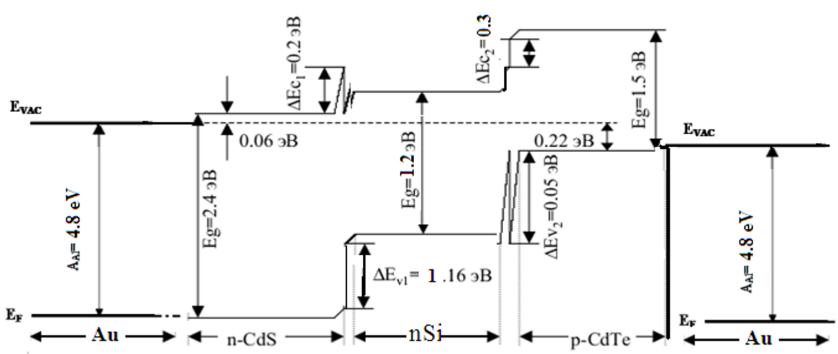


Fig. 7. Energy band diagram of the Au-nCdS-nSi-pCdTe-Au structure in the equilibrium state

It is obvious that the introduction of films of chalcogenide compounds CdT e and CdS into the active region of the diode leads to the following results:

firstly, there is an expansion of the spectral range of photosensitivity into the near-IR region below the optical absorption edge of silicon to 1.4 µm, which corresponds to the optical band gap for films of chalcogenide compounds CdTe and CdS at room temperature 300 K [18]; secondly, the photoresponse in this region has increased by more than two orders of magnitude, including at wavelengths corresponding to the transparency windows of quartz optical fibers, which are used for telecommunications;

Thirdly, there is an almost tenfold increase in sensitivity near and above the band gap of Si in the region $\lambda = (1.0 \div 1.4)$ µm, which is also associated with the contribution to photon absorption and carrier generation in films of chalcogenide compounds CdTe and CdS.

Therefore, the external potential applied to the structure, including the contact potential difference, mainly falls on the space charge layer of the structure boundaries. Moreover, surface states (N_{SS}) at the interface of contacting semiconductors - cadmium sulfide and silicon, can affect the height of the potential barrier. The nature of these surface states is associated with the difference in the crystal lattice constants n CdS and n Si, as well as p CdTe and n Si. The properties of the multilayer diode structure of Au - n CdS-nSi - p CdTe-Au heterojunctions depend on the technological parameters and method conditions.

4 Results and discussion

The results obtained from the study of the VCC of a multilayer photodiode Au - nCdS - nSi - pCdTe - Au - structure show that the thickness of the space charge narrows in forward bias, and in reverse, it expands with increasing bias voltage. In addition, the space charge resistance is the determining resistance of the entire structure, since the nCdS layer in heterostructures is a high-resistivity and highly compensated material, as evidenced by the fact that the structures belong to semiconductor MIS structures. From the dark and light current-voltage characteristics, it is determined that charge carriers generated by radiation when illuminated by a filament lamp with a power of 100 W are separated by the field of a multilayer heterojunction nSi - p CdTe and n CdS-nSi.

The conducted studies show that the current-voltage characteristic of Au-nCdS-nSi-pCdTe-Au structures has three sections: power-law - $I \propto V^{2.44}$, sublinear $V \propto \exp(Jad)$, and prebreakdown dependence – $I \propto V^{5.55}$, arising in nCdS-nSi-pCdTe layers with a change in current density at a constant temperature due to a change in the type of recombination processes. Recombination of nonequilibrium carriers at low current densities occurs through point local centers (defects), and at high current densities, complex complexes are responsible for the recombination processes, within which electron exchange occurs. Based on the data obtained, it was established that in the layers nCdS-nSi - pCdTe photosensitive Au - nCdS - nSi - pCdTe - Au structure, impurity complexes (defects) are formed, in which the rate of recombination of nonequilibrium carriers at low excitation levels is determined by simple local centers in the boundary transition layers. A band diagram of a multilayer photodiode structure Au - nCdS-nSi - pCdTe - Au has been constructed, which can be schematically described as Au - nCdS + nCdS - nSi + nSi – pCdTe + pCdTe - Au.

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