MINIATURISED INTEGRATED CIRCUIT CORE ELEMENT FOR POINT OF LOAD (POL) CONVERSION

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ABSTRACT

In the last years Point of Load converters (PoL) appeared as a clear bottleneck for the realisation of digital applications for space (to supply FPGA's, microprocessors, memories, specialised digital circuits, etc.). Many preparatory activities have been conducted by ESA to define a target specification, taking into account promising European technologies and user's requirements. This paper provides a brief technical description of a PoL IC device designed and manufactured by STMicroelectronics and shows the main test results and performances in order to demonstrate that this integrated solution embeds the most important features that a Point of Load (PoL) device should have. The device is the outcome of a design activity executed in relation to the TRP activity entitled "Miniaturised core element for Point of Load (PoL) conversion" (T703-305EP of the TRP work plan 2011-2013). The realization of this product enables STMicroelectronics to compete in the global world market, since this is a prerequisite for the future availability of PoL products, for their commercial success and their sustainability.
An export licence-free, performing and advanced PoL ASIC (Application Specific Integrated Circuit) would be a major achievement.
It would encounter interest from users and would resolve the problem of supplying digital loads with the required accuracy and dynamical performances.

1. INTRODUCTION

Typical switching Point of Load ASICs, used in distributed power conversion terrestrial systems and in those applications requiring low power dissipation, are generally sensitive to radiation effects, both Total Dose and Single Event Effects. Today a variety of commercial switching DC-DC converters are available from many American & European suppliers (including STMicroelectronics), but European manufacturers and suppliers are mainly oriented in developing products towards industrial, automotive, computer peripheral and consumer applications rather than for space applications.
At the moment mainly non-European suppliers are providing RH or Rad-tolerant PoL converters for space applications. Some of these devices are QML qualified and are procurable according to an electrically screened SMD. This represents a potential risk to the European space industry, as these MIL qualified devices are subject to US export licenses and/or US Department of Commerce rules. Obviously, under the given policy constraints and commercial conditions associated with the U.S. source, the development of a European supplier alternative is expected to result in significant cost and schedule advantages.
Project's objective from STMicroelectronics was to design, develop and manufacture a European HI-Rel, Rad-Hard Point of Load (PoL) core and is supported by ESA and National Space Agency. The Point of Load ASIC (hereafter called RHFPOL01) is suitable for an extensive range of Space applications (meteo, communication, earth observation satellites) including those ones with mission durations in the range of 15-18 years. STMicroelectronics is committed to get a product for the worldwide space customers, which implies primarily QML-V qualification and the insertion to the European Preferred Part List. ST will be open to discuss also the additional ESCC Evaluation and Qualification providing specific support.

2. RHFPOL01 ASIC

The RHFPOL01 device is a radiation hardened, high efficiency, monolithic, synchronous step-down switching regulator with high precision internal voltage reference and integrated power MOSFETs for synchronous conversion. The device is developed using ST built-in SOI (Silicon On Insulator) technology that offers excellent performance against SEL (Single Event Latch-up) effects. The regulator converts the input

voltage V_{IN} in the range [3.0V ÷ 12V] to output voltage V_{OUT} from 0.8V up to 0.85xV_{IN} and is able to provide up to 7A output current. In Fig.1 a typical application is shown in which the RHFPOL01 device is embedded.

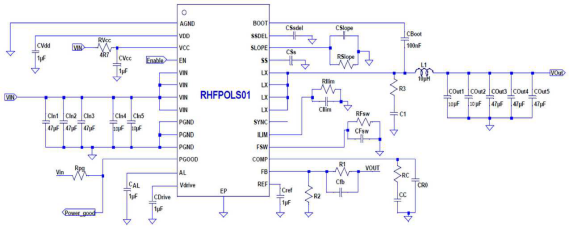

Figure 1 - RHFPOL01 Application Circuit

The major application fields for this device are:
- Point of load regulation for space applications
- FPGA, DSP, CPU and ASICS supply for space applications
- Low-Voltage, High-Density Distributed Power Systems

2.1 RHFPOL01 Block Diagram & Features

The block diagram of RHFPOL01 is shown in Fig. 2. The controller is based on peak current mode control loop architecture which, with its embedded error amplifier and external compensation, enables a stable operation with a wide range of output filter configurations (including Multi-Layer Ceramic Capacitor – MLCC- solutions) ensuring fast response to load transient and very stable switching frequency. The fault management consists of output over-voltage protection (not-latched) and latched/auto-recovery over-current and thermal protections.

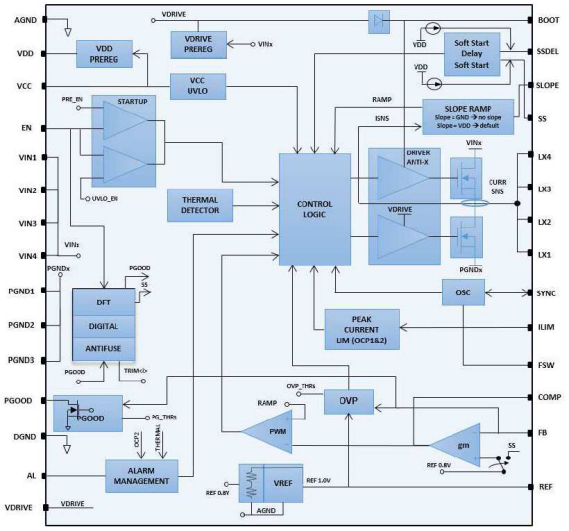

Figure 2 - RHFPOL01 Block Diagram

Low R_{DS_ON} N-channel MOSFETs are used for both HS (high-side) and LS (low-side) switches and also the bootstrap MOSFET driver diode is embedded, for minimum external components provision.

2.2 Start-up and soft-start

The dedicated enable (EN), programmable soft-start (SS) and soft-start delay pins (SSDEL) offer an easy control on the power sequencing and inrush current. Once V_{CC} voltage is above the V_{CC_UVLO} rising threshold, the device waits for enable pin (EN) assertion and then begins the soft-start. In order to add flexibility to turn-on management, the enable pin (EN) has two thresholds: if EN < 0.7V, the IC is fully OFF and the current consumption is typically 400µA. If EN > 1.24V the regulator starts switching, after the SSDEL time elapses. When EN pin is kept between the two thresholds, the main blocks of the regulator are turned ON and the RHFPOL01 device is ready to start regulation. It should be noted that the external filtering capacitors connected between function programming pins (FSW, ILIM and SLOPE) and GND (as shown in Fig. 1), have a direct impact on the IC wake-up timing. In order to be sure that the soft-start sequence starts only when the functions programming pin voltage is stable, the soft-start delay (SSDEL) has been added. The typical start-up sequence is depicted in Fig. 3.

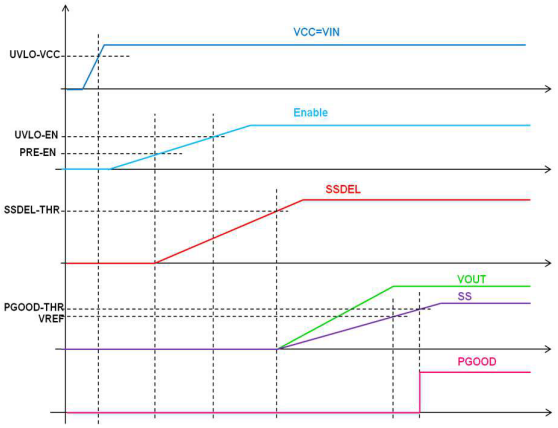

Figure 3 RHFPOL01 start-up sequence

During start-up phase, in order to prevent in-rush current when the V_{OUT} voltage is too low, two switching frequency changes are implemented. This feature is clearly shown in the Fig. 4 (assuming a final programmed frequency of 500 KHz).

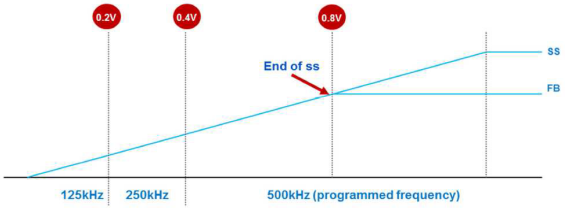

Figure 4 - Switching frequency changes during start-up

As long as voltage on pin SS is < 0.2V, the switching frequency is ¼ of programmed frequency. When SS

value is between 0.2V and 0.4V the switching frequency is ½ of the programmed frequency. After SS reaches 0.4V, the switching frequency nominally reaches the programmed one.

2.3 Control loop

The simplified block diagram of RHFPOL01 control loop is shown in Fig.5. It consists in a constant-frequency peak current-mode control and employs two control loops: an external loop to control the output voltage and an inner loop to control the peak current which flows through the coil. The external loop (voltage loop) compares the feedback voltage V_{FB} with the internally generated precise 0.8V reference voltage through the error amplifier EA.

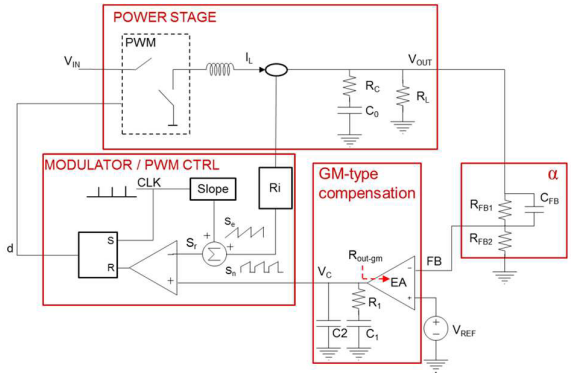

Figure 5 - RHFPOL01 Control Loop

The error amplifier EA is a trans-conductance amplifier (OTA) that, starting from the difference between reference and feedback voltages, adapts the voltage level on node V_C (pin COMP), where external RC compensation network is connected, in order to provide the proper regulation. In the inner loop (i.e. current loop), the current sense circuit converts the current flowing through the coil into a sense voltage Sn according to the gain factor R_i. In addition, the voltage ramp Se, programmable by the external R_{SLOPE} resistor, is added to the Sn signal to get stable operation in case of duty cycle greater than 50%. The voltages V_C and the resulting ramp Sr (see Fig. 5) are compared by means of a PWM comparator and a Pulse Width Modulated (PWM) signal is generated, defining the duty cycle d. The power stage can be seen as a controlled current generator, which provides the current I_L to the power stage output capacitor and load.

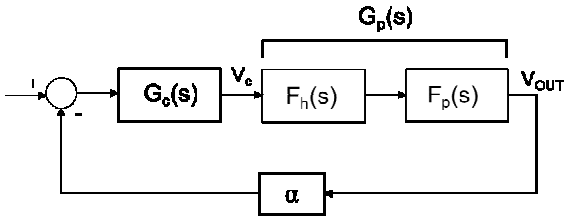

Figure 6: RHFPOLS01 control loop function

Complete small signal model of the converter is obtanined according with PWM switch model, proposed in [3], and small signal model of the peak current mode, proposed in [4]. By combining the open loop transfer function with the compensator and the feedback network, the closed loop transfer function is obtanied:

$$G_{loop}(s) = \alpha(s) \cdot G_p(s) \cdot G_c(s) \qquad (1)$$

Where:

$$G_p(s) = G_p(0) \cdot \frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)} \cdot \frac{1}{1+\frac{s}{\omega_n Q_p}+\frac{s^2}{\omega_n^2}} \qquad (2)$$

$$G_C(s) = g_m \cdot R_{out\_gm} \cdot \frac{\left(1+\frac{s}{\omega_{zc}}\right)}{\left(1+\frac{s}{\omega_{pc1}}\right)\cdot\left(1+\frac{s}{\omega_{pc2}}\right)} \qquad (3)$$

$$\alpha(s) = \frac{R_{FB2}}{R_{FB2}+R_{FB1}} \cdot \frac{\left(1+\frac{s}{\omega_{zcfb}}\right)}{\left(1+\frac{s}{\omega_{pcfb}}\right)} \qquad (4)$$

Equations of first order pole and zero of the output filter are:

$$\omega_Z = \frac{1}{R_C \cdot C_O}; \qquad (5)$$

$$\omega_P = \frac{1}{(R_L+R_C)\cdot C_O} + \frac{T_S}{L \cdot C_O}\left(m_C \cdot (1-D) - \frac{1}{2}\right) \qquad (6)$$

The second order term in the equation (2) gives double pole at half of switching frequency. The equation (3) represents the contribution of GM-type compensation network. The relative zero and two poles are below:

$$\omega_{zc} = \frac{1}{R_1 \cdot C_1}; \quad \omega_{pc1} \cong \frac{1}{R_{out\_gm} \cdot C_1}; \quad \omega_{pc2} \cong \frac{1}{R_1 \cdot C_2} \qquad (7)$$

Finally, the feed-forward capacitor add pole-zero factor α spaced:

$$\omega_{zcfb} = \frac{1}{R_{fb1} \cdot C_{fb}}; \quad \omega_{pcfb} = \frac{1}{C_{fb} \cdot \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1}+R_{FB2}}} = \frac{\omega_{zcfb}}{\alpha} \qquad (8)$$

Generally, R1 and C1 are chosen to compensate the pole due to the output capacitor.

To improve the response of the converter up to 75% of step load, the EA is designed to have not-linear g_m for large input offset. Here below measurement result of the gm versus the feedback voltage is shown.

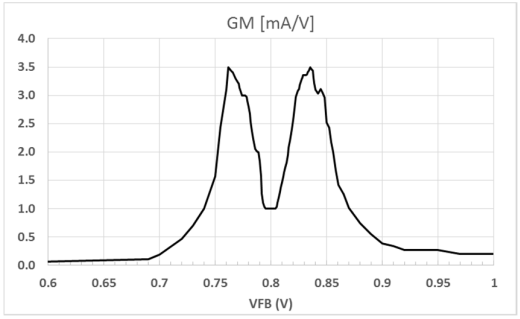

Figure 7: Error amplifier trans-conductance.

2.3.1 Stability, phase and gain margin vs model

To evaluate in detail the stability of the converter, a proper estimation of poles and zeros must be obtained according with internal circuitry tolerances, output capacitor variation and compensation network. Dedicated model is provided by ST in worksheet format to help the final user on choosing proper compensation elements. For instance, a comparison between test bench measurements and the model is shown in Fig. 8 and Fig. 9.

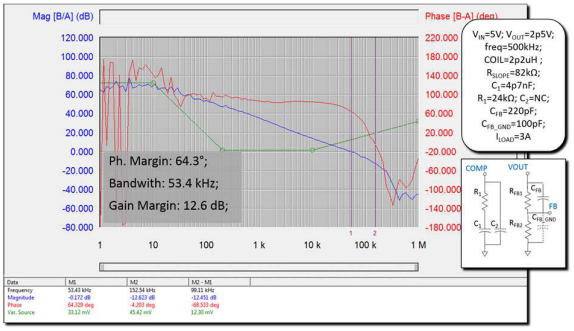

Figure 8: Stability and open loop measurement

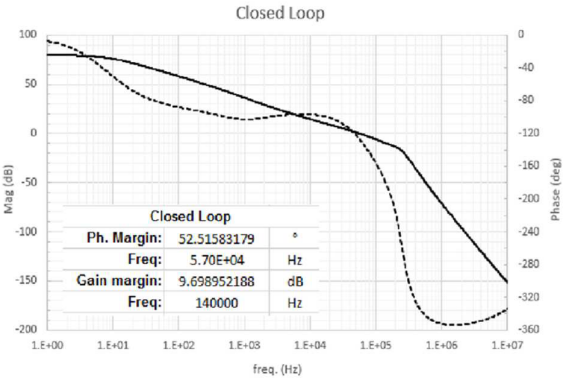

Figure 9: Stability and open loop worksheet result

2.4 Fast load transient response

When fast load transient is applied to the output, the device is able to react very quickly in order to limit output voltage overshoot or undershoot. This feature is implemented by the combination of a fast error amplifier response and a proper control logic scheme that is driven by the use of two fast comparators, called HL (High Load) and LL (Low Load). When the voltage FB goes below the HL reference point REF_HL (see Fig. 10), the HL comparator forces ON the HS power switch. Typically, REF_HL level is -5% below the nominal voltage loop reference of 800mV. The HL comparator output remains latched to high level voltage until the programmed current limit is reached or the output voltage goes back into the linear control regulation voltage level. So, a proper voltage hysteresis is implemented: the comparator output goes low when the feedback goes back again to -2.5% of the regulation threshold (see Fig.10). If during the ON phase current limit is reached, minimum OFF time period around 200ns is applied.

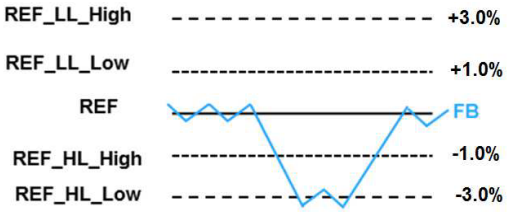

Figure 10 - Fast Load Transient Response

In opposite way, when the load current quickly decreases, the FB voltage can show an overshoot. The LL comparator output goes high when the FB goes above the LL reference point voltage REF_LL (typically +7% above the nominal 800mV reference) and an OFF time is forced. The OFF time is kept till either the FB goes back to the hysteresis threshold (typically +2.5%) or a negative inductor current threshold is reached. In fact, the device naturally works in full PWM mode, but when fast negative step load occurs, the current on the coil can quickly go below zero. So, a zero crossing comparator, with a typical threshold of -1.5A, is implemented avoiding the inductor coil goes deeply below zero. When the zero crossing threshold is reached, switching activity is stopped and the power stage is forced in open loop condition (point LX is in high impedance). Of course, the two comparator themselves are not enough for a smooth operation but, as mentioned above, they also need the concurrent action of the error amplifier. A fast error amplifier with dynamic bias has been designed in order to improve the load-transient response. In practice the error amplifier must be able to quickly charge or discharge the compensation capacitor (on pin COMP) changing its output in non-linear shape at a step change in the input of the error amplifier itself. So, when one of the two comparators drives ON or OFF time, in parallel the bandwidth and the large signal current capability (including the large signal current gain) of the error amplifier are increased. Finally, this solution allows a fast load transient response with lower output capacitance and smaller output voltage drop.

2.5 Synchronization & Interleaving

Two RHFPOL01 ASICs can be configured in Master and Slave mode. The clock synchronization is realized configuring one IC as Master (with a proper switching frequency) and the second IC as Slave, shorting its pin FSW to GND and by connecting together the pin SYNC of each device. When the device is the MASTER its pin SYNC is configured as clock output and gives out the internal switching clock frequency with a 180° phase shifting. If the device is a SLAVE its pin SYNC is configured as clock input, and the device uses the clock received on pin SYNC to synchronize its internal switching clock.
In synchronized mode, each device will have its own output and compensation network (see Fig. 11a), while in the interleaved configuration the two devices share the same output and compensation network (see Fig. 11b). The main benefits of interleaved configuration are a doubled capability of output current and the reduction of RMS current absorption from the input filter, preventing beating frequency noise and therefore allowing a reduction in the size and cost of the input filter, at equal ripple conditions.

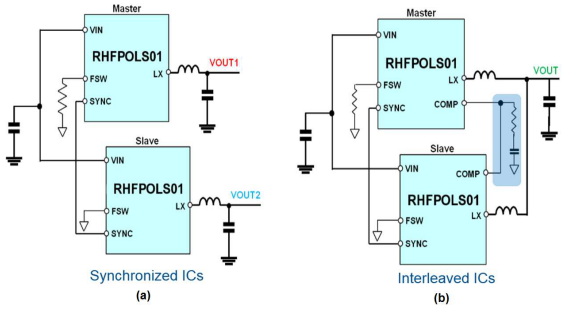

Figure 11 - RHFPOL01: Synchronized & Interleaved ICs

The Fig.12 shows the experimental result of two RHFPOL01 ICs that are working in interleaved configuration providing up to 14A output current.

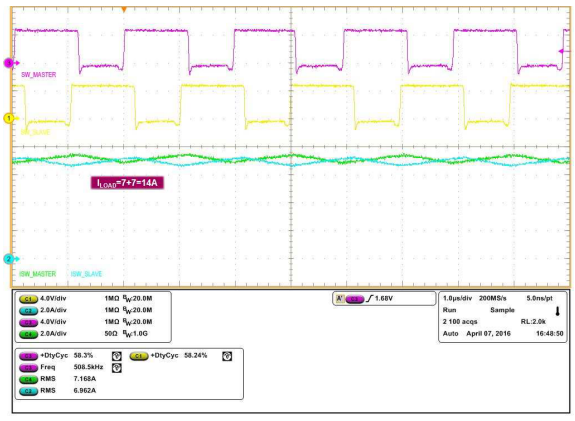

Figure 12: Measure on two interleaved ICs

To guarantee uniform heat distribution and balancing of the electrical stress between the two devices, the total output current I_{LOAD} is shared inside each device (I_{OUT1}, I_{OUT2}) with an accuracy of 10%. It means that:

$$I_{OUT1,2} < I_{LOAD}/2 \pm 10\% \qquad (9)$$

A brief description of the approach used to guarantee the load sharing accuracy is shown in Fig. 13. Shorting together the nodes COMP_M (master) and COMP_S (slave) and also trimming both internal current sensor and slope circuitries, a good accuracy will be ensured.

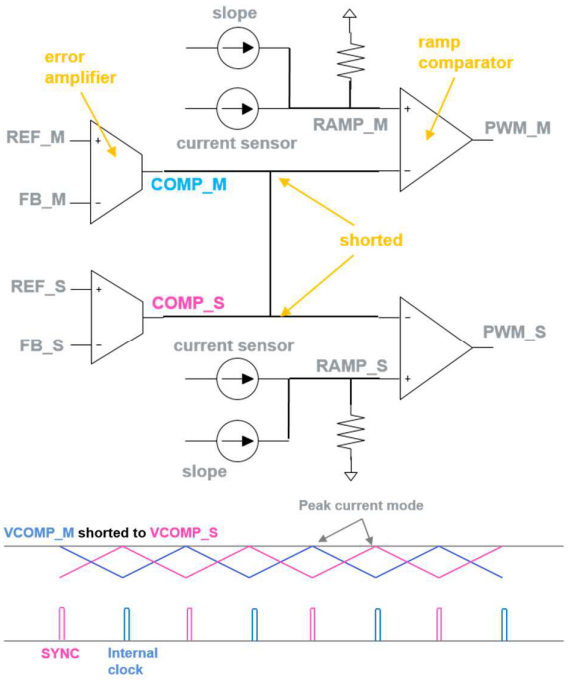

Figure 13: Block diagram and signals for load sharing

It can be interesting to highlight that a strength of this approach is that, slightly changing the value of the external R_{SLOPE} resistor, a fine tuning of final accuracy is possible. In this way, possible asymmetries (due to coil, board resistive paths …) can be recovered and the accuracy can be improved.

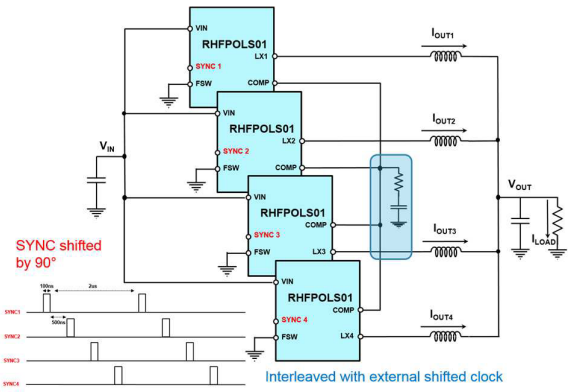

Figure 14: four Slave Interleaved ICs at 500 kHz

To increase even more the output current capability, it is

possible to connect more than two devices ("*n*" in general) in interleaved configuration. In this case, in order to guarantee a proper phase shifting (360°/*n*), all the devices are configured as slave and then an external clock signal must be provided to each device.
In Fig.14 is shown a configuration with four slave devices connected in interleaving mode able to provide up to 28A (here phase shifting is 90°, of course).
Also in this case the load sharing accuracy is guaranteed:

$$I_{OUT1,2,3,4} < I_{LOAD}/4 \pm 10\% \qquad (10)$$

To perform this measurement in our lab, two dedicated boards for double load sharing were connected in parallel, as shown in the figure below.

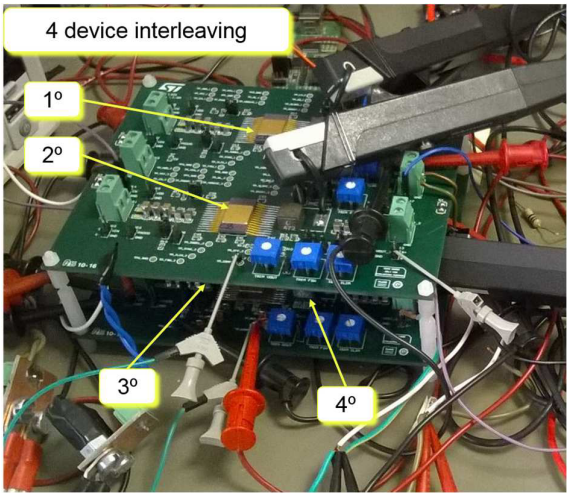

Figure 15: Board equipment of four Interleaved ICs

Even if the resistive paths have not been optimized, the final accuracy was in spec, as can be seen in the measurements highlighted in Fig.16:

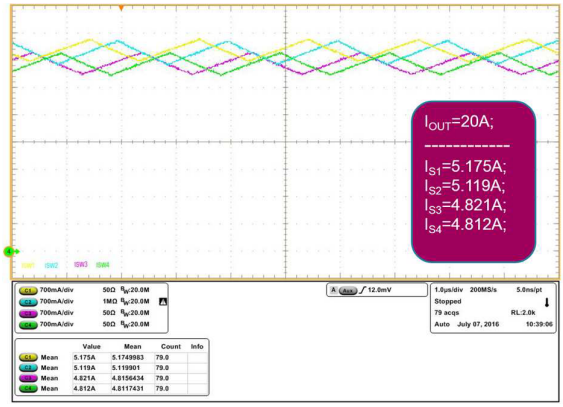

Figure 16: Measure of four Interleaved ICs

2.6 RH_OTP and Run Trimming

The RHFPOL01 embeds a radiation hardened OTP (One Time Programmable circuit, realized with anti-fuse cells) that gives the final user the possibility of tuning the accuracy of some key parameters (such as V_{OUT}, Freq, Ilim…) directly on the application board and during the device regulation, practically like a "run trimming". In this way, the final accuracy will be higher because also the effect of the external passive elements (FB resistor, external resistor to set frequency…) will be compensated during measurement and trimming operation.
The "Run Trimming" consists of two phases: the simulation and the burning phases. During the simulation phase, the user can choose the best trimming value by using the dedicated software and hardware that implement i2c (Inter Integrated Circuit) communication protocol. After trimming the pattern is verified by simulation phase and the final user can proceed with the final burning phase. The figure below depicts the Run Trimming for V_{OUT} parameter performed during the normal switching activity of the device.

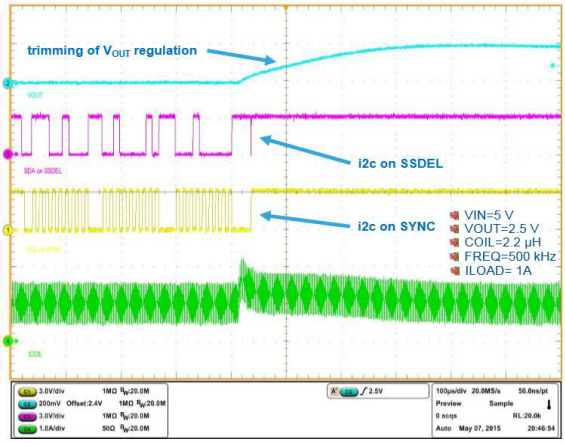

Figure 17 - RHFPOL01: V_{OUT} Run Trimming

2.7 Protection and Alarms

The RHFPOL01 device features a full set of protections and output voltage monitoring:

- PGOOD (power good function) realized by means an open drain output at pin PGOOD, which is externally pulled-up to VIN if the output voltage is in ±10% of regulation window. During start-up, turn-off and fault detection the PGOOD pin is forced low.
- OVP - Over Voltage Protection: The output overvoltage protection is triggered as soon as the output regulated voltage exceeds +25% of the nominal value.
- ILIM1: 1st level of over current protection.
- ILIM2: 2nd level of over current protection.
- OVTP - Over Temperature Protection. The strategy used for this kind of protection took into account that it is required (by ECSS derating rules) that Si devices never exceed the maximum allowable junction temperature of 110ºC (in steady state operation), or up to the rated limit for transients. The RHFPOL01 implements the following thermal shutdown feature:

when the junction temperature reaches 155ºC the device turns OFF both internal MOSFETs and then pin PGOOD is forced low. When the junction temperature drops again to around 135ºC, a delay time on pin AL elapses before the device restarts with a new soft-start sequence (see Fig.18).

The OVP and ILIM1 alarms are non-latching alarms. They put the device in T_{OFF} (ILIM1) or in high impedance conditions (OVP) but the regulation continues normally when the alarm condition elapses.
The ILIM2 and OVTP alarms are managed in a more complex way. A programmable waiting time (cooling window) and a proportional watchdog window are implemented according with the value of the external capacitor (C_{AL}) connected to pin AL. In this way the user has the possibility to manage the cooling of the chip (through the waiting time) and to distinguish if there is a persistent alarm condition or not (through the watching window). For both ILIM2 and OVTP protections, the RHFPOL01 can be configured in "Latched" or "Hiccup" operation mode in case of persistent events. For thermal alarms, if Latched or Hiccup mode is desired, the value of C_{AL} must be carefully chosen to select a watching window duration respectively longer or shorter than the time required by the device to trigger the thermal protection after the cooling time is elapsed. In the figure below is shown the Latched OVTP protection in case of 16 consecutive thermal events: note that in this case the over temperature condition can only appear as a transient one and cannot be indefinite, respecting the above mentioned ECSS derating rules.

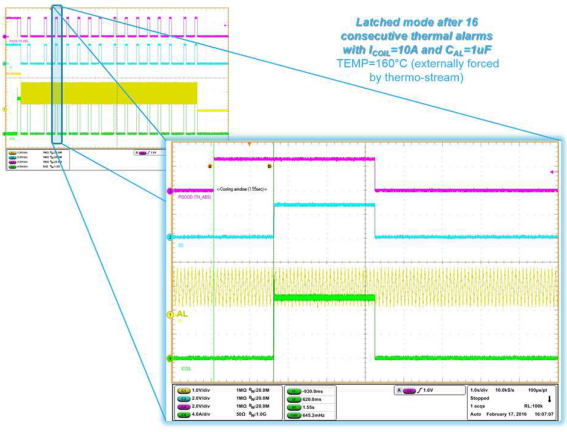

Figure 18 - RHFPOL01: Latched mode OVTP

2.8 RHFPOL01 Efficiency and Current Capability

Several efficiency measures have been performed on the silicon at different V_{IN}/V_{OUT}, switching frequency and inductor values, matching the expected target. In the figures below some experimental results are reported:

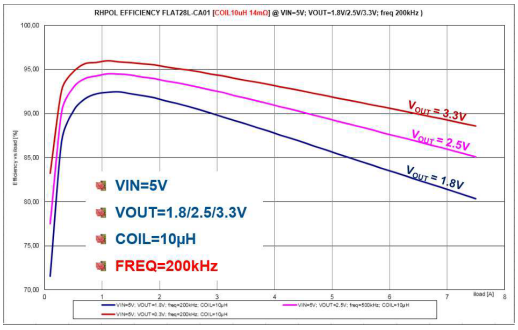

Figure 19 - RHFPOL01 Efficiency @ different V_{OUT}

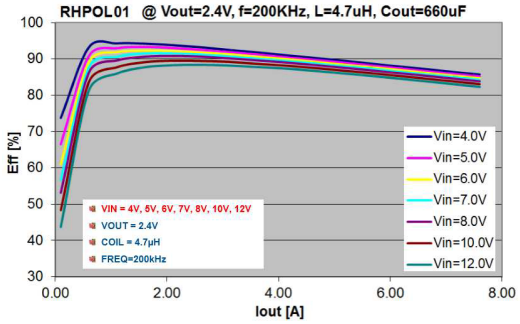

Figure 20 - RHFPOL01 Efficiency @ different V

Test performed in our lab showed that the RHFPOL01, mounted in the official FLAT28L hermetic ceramic package, is able to provide a current capability well above its project target of 7A. In fig.21 the result of an experimental test is shown during which the device provides an output current of 10A. By means of a thermal camera, in this condition we were able to measure a Pack temperature value of 110°C.

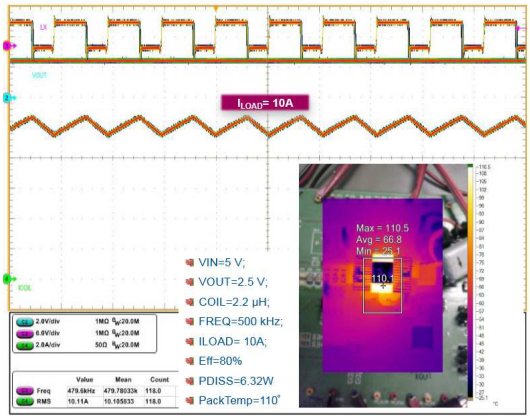

Figure 21 - RHFPOL01: Output Current Capability

2.9 RHFPOL01 Application Boards

In order to evaluate all the technical features of RHFPOL01 device, a very versatile Evaluation Board (shown in Fig.22) has been realized. Of course, this board has to be used for debug and evaluation purposes only and then it was not optimized in terms of

dimensions and count of external components. In addition (see Fig. 16), a dedicated application board for the current sharing feature has been also manufactured, in order to optimize the symmetry that is required for this kind of application test.

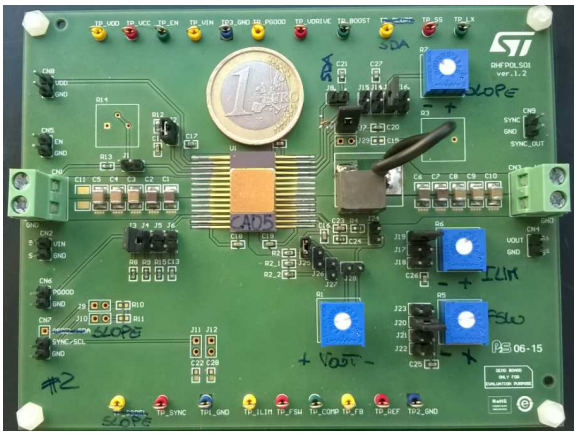

Figure 22 - RHFPOL01: Evaluation Board

Finally, a dedicated demo-board is under manufacturing (at the time of this paper) with the aim to exalt the key technical features of RHFPOL01 device (like the transient response and the system efficiency) through the choice of a proper setting and by minimizing the count of external components and PCB dimensions.
The top view and the real dimension of this demo-board are depicted in Fig. 23.

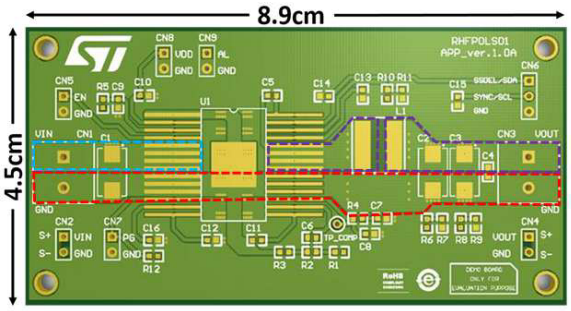

Figure 23 - RHFPOL01: Demo Board

The resulting pin-out of RHFPOL01 device was thus the best trade-off between the minimization of parasitic effects of FLAT28L package and the need to avoid complications in the layout of application boards. In Fig.23 are highlighted the paths involved in the power distribution.

3. PSPICE model

To allow a better customization of final application the PSPICE macro-model including all the main features of RHFPOL01 is already available. Comparison tests between the silicon and PSPICE model have been performed with good results as the one shown in Fig. 24 describing the behaviour of the device at start-up.

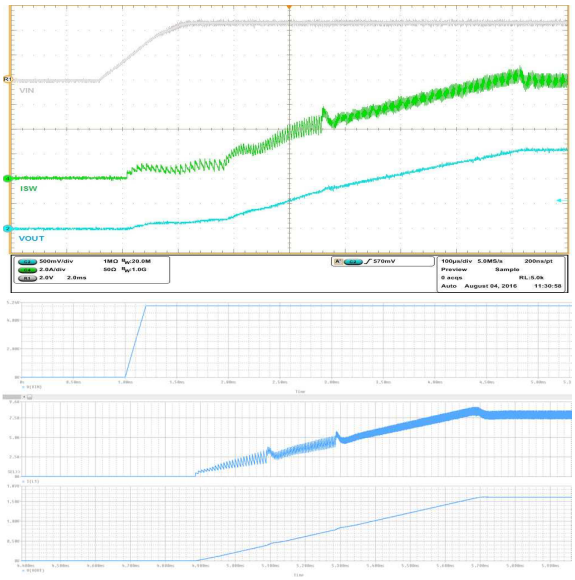

Figure 24: Simulation comparison Silicon vs PSPICE

In this way, the final user can explore the behaviour of its system before to realize the final application board.

4. RADIATION TARGET

The final product must be able to survive in harsh conditions that are different for each orbit assigned to satellites. The key radiation targets are:

- Operate in the Mil-Temperature range (-55°C to +125°C);
- To be robust in radiation (total ionizing dose) up to 100 krad (Si) at standard exposure rate (i.e. 50rad/sec) and low dose rate (i.e. 0.01 rad/sec);
- To be robust in radiation (SEE) up to 70 MeV/mg/cm2 LET, SEU and SEL immune, not affected by SEGR or SEBO and not suffer from appreciable performance degradation to SET.

Preliminary TID radiation tests (HDR & LDR) have already been successfully performed on RHFPOL01 prototype up to 300 krad(Si) at high dose rate (11.4 krad(Si)/h) and up to 100 krad(Si) at low dose rate (0.1 krad(Si)/h) using gamma rays from Cobalt-60 source.

5. REFERENCES

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3. V. Volperian, “Simplified analysis of PWM converters using model of PWM switch part I: continuous conduction mode”, IEEE Trans. On Power Electronics, vol. 26, no.3 pages 490-496.
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