HIGH POWER SELF-ALIGNED, TRENCH-IMPLANTED 4H-SiC JFETs**K. Vamvoukakis⁽¹⁾, A. Stavrinidis⁽¹⁾, D. Stefanakis⁽¹⁾, G. Konstantinidis⁽¹⁾, M. Kayambaki⁽¹⁾, K. Zekentes^(1,2)**⁽¹⁾ IESL/ FORTH, Vassilika Vouton, PO Box 1385 Heraklion, Greece

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⁽²⁾ Grenoble-INP, IMEP-LAHC, F-38000 Grenoble, France Email: konstantinos.zekentes@imep.grenoble-inp.fr**ABSTRACT**

The process technology for the fabrication of 4H-SiC trench-implanted-gate 4H-SiC vertical-channel JFET (TI-VJFET) has been developed. The optimized TI-VJFETs have been fabricated with self-aligned nickel silicide source and gate contacts using a process sequence that greatly reduces process complexity as it includes only four lithography steps. A source-pillars sidewall oxidation and subsequent removal of the metallization from the top of the sidewall oxide ensured isolation between gate and source. Optimum planarization of the source pillars top has been performed by cyclotene spin coating and etch back. The effect of the channel geometry on the electrical characteristics has been studied by varying its length (0.3 and 1.2 μm) and its width (1.5-5 μm). The voltage blocking exhibits a triode shape, which is typical for a static-induction transistor (SIT) operation. The transistors exhibited high ON current handling capabilities (Direct Current density $>1\text{kA}/\text{cm}^2$) and values of R_{ON} ranging from 6 - 12 $\text{m}\Omega\cdot\text{cm}^2$ depending on the channel length. Maximum voltage blocking was 800V limited by the edge termination. The maximum voltage gain was 51. Most transistors were normally-on. Normally-off operation has been observed for transistors lower than 2 μm channel width (mask level) and deep implantation.

1. INTRODUCTION

Power transistors based on wide band gap semiconductors are subject of intensive research the last decade. The high current and high voltage capabilities of these devices, largely exceeding that of Si devices, represent a challenge on various aspects related to the device fabrication, characterization and packaging.

Currently, SiC and GaN are the wide band gap semiconductors of choice for fabricating high power devices. SiC is more appropriate for high voltage ($>1000\text{V}$) applications and more mature from the technology point of view as many devices are commercially available. For instance SiC devices exhibit 6 times higher current density at 600 V [1].

4H-SiC-based Metal-Oxide Semiconductor Field-Effect Transistor (MOSFETs), Bipolar Junction Transistors (BJTs) and JFETs have been considered as candidate devices since their technology is more mature than other transistor types.

All things considered, the MOSFET is the most promising device in the SiC field [2]. Its technology is more mature, it is a normally-off device and with little demand on the drive circuits. However, reliability issues (oxide and threshold voltage stability) were the main obstacles for their commercial release despite the long and important effort devoted towards their optimization. Reliability is a minor issue in the commercial devices but it becomes a major one when these devices are considered for space applications.

The SiC BJT main advantages as power switch are its low conduction loss combined with fast switching. Moreover, BJTs are generally very robust devices meeting in many cases space requirements. The most crucial parameter for SiC BJT optimization was the current gain at application temperature. Current gain values lower than 30 were obtained for a long time by various research groups. This issue has been addressed successfully by performing special surface passivation based mainly on oxides [3]. Again, there is a high risk that this surface passivation will not be effective under space conditions.

JFETs have the lowest overall losses of switching devices and their fabrication process is quite straight forward. The main drawback with VJFETs is that they are usually normally-on (depletion mode), which is considered unsafe in power applications. Moreover, JFETs are very robust devices with a channel not seriously affected from surface effects. There is no a major issue up to the moment limiting their application in space conditions. This was the reason for developing SiC JFETs at FORTH.

Once the main device type has been chosen, the next question is to choose the appropriate JFET geometry. The usual 4H-SiC JFETs are either purely vertical (VJFETs with Static Induction Transistors-SITs operation) or Semi-lateral (SLJFET). Optimum SLJFET fabrication requires two-step implantation and re-epitaxial growth after material etching on specific locations. Trenched VJFET requires only one implantation step and the less lithography steps. The only difficulty is the tight control of the dimensions, which are of the order of 1-2 μm for both source pillars and gate pitch arising, thus, an issue of tight registry control. For the above reasons, the trenched and implanted TI-VJFET has been chosen as optimum device.

The 4H-SiC VJFETs/SITs have been developed during the 90's and early 00's [4] for microwave applications and are incorporated in radar systems. High power 4H-SiC SITs with excellent high power performance have been demonstrated later [5, 6] and an excellent review is given in [7].

The purpose of the present study was to thoroughly investigate all 4H-SiC SITs process steps with the ultimate goal to simplify as much as possible their fabrication. Towards this aim different lithographic approaches, metallization schemes, isolation dielectrics and gate implantation conditions have been tested. This effort resulted in the fabrication of SiC TI-VJFET with self-aligned nickel silicide source and gate contacts including only four to six lithography steps depending on the edge termination scheme.

Figure 1. Schematic of the device cross-section.

2. DEVICE PROCESSING

The cross-section of the optimized 4H-SiC TI-VJFETs is shown in Fig. 1. The current flows vertically through

an array of the source “pillars”, which is controlled from the P-type implanted gate trench areas between each pillar.

A series of optimization runs have been performed in order to choose this structure. Different epitaxial structures and gate implantation geometries were used. The epitaxial structure corresponding to Fig. 1, was composed by a 8 μm (L_{dr}) blocking thick n-layer with $N_D=5\times 10^{15}\text{ cm}^{-3}$, an 1.2 μm ($L_{ch}+L_{pchan}$) channel layer n-layer with $N_d=1\times 10^{16}\text{ cm}^{-3}$ and a top 1 μm (L_{pcont}) thick n+ layer with $N_d=1\times 10^{19}\text{ cm}^{-3}$. Gate regions were formed by Al ion implantation and post-implantation annealing (see details below) resulting in an implanted layer with p-type doping of $1\times 10^{19}\text{ cm}^{-3}$. Two different implantation depths ($L_G=0.3$ and 1.1 μm), have been employed. The two transistor types will be distinguished by mentioning them as the “short” and “long” channel VJFET.

The technology of 4H-SiC SITs are simpler than that of MOSFETs or BJTs and the main difficulty lies with the small width ($\sim 1\mu\text{m}$) of the source pillars requiring the use of advanced photolithography equipment (steppers, e-beam lithography) or self-aligned approach in the case of contact lithography. Indeed, our initial tests with conventional contact lithography showed its limitation not allowing the fabrication of structures with small channel widths a necessary condition for high voltage blocking in this type of devices.

The main issue in the case of the self-aligned process is related to the metal tears and wings, which should be avoided in order to have a large gate-source breakdown. In the case of Fig. 2(a) these features are not excessive but a study, relative to the use of different photoresists, allowed eliminating them completely (Fig. 2c).

Source fingers and gate trenches were formed by reactive ion etching (RIE) by using the first lithographic step.

Gate regions were formed by ion implantation followed by a thermal annealing at 1600-1800 $^{\circ}\text{C}$. The same multilayer metal mask was used to perform the above RIE etching and form gate regions by ion implantation. Aluminium was implanted at temperature of 425 $^{\circ}\text{C}$ with normally incident ion beam (sample's surface and ion beam are perpendicular). Individual implantation

Figure 2. Source pillars after metallization deposition in the case of non-optimized self-aligned (a) conventional-contact-lithography (b) and optimized self-aligned (c) processes.

energies and fluencies were calculated using the SRIM 2D simulation program to form the Al profile. The gate profile has been checked by Secondary Ion Mass Spectroscopy (SIMS) performed on as-implanted and as-post-implantation-annealed witness samples.

The effect on the surface morphology of the SiC-surface-coverage by a C-cap during the post-implantation annealing, is obvious from Fig. 2 as a step-bunching is observed in the case without C-cap (Fig. 2b&c) despite the fact that an optimized process based on SiH₄ overpressure has been used. Indeed, trying to use SiH₄ overpressure to avoid dopant redistribution and surface step bunching is a tricky process because it can result easily to a Si deposition on top of SiC material. Therefore, the use of C-cap is the optimum solution.

Following, a 50 nm thick Ni contact is deposited by e-beam evaporation and patterned (second photolithography step) to remove the metal from the edge termination and device separation regions. Nickel has been chosen as metallization on both source and gates as it results to lowest contact resistance in the case of n-type SiC. Al-based metallizations result in lowest contact resistance in the case of p-type material. However, obtaining a low contact resistance on source n-type material is crucial for low device losses and for this reason Ni was our choice.

Nickel is deposited in a self-aligned way on both source pillar tops and gate trenches (Fig.2). In this way, Ni is deposited on the edge of the pillar tops i.e. on top of the thermal oxide and quite probably on the pillar sidewalls.

Figure 3. SEM images taken (a) after RTA at 1000°C, (b) after BCB deposition and etch-back from the source fingers and (c) after 2nd etch-back on the gate pad.

A study on optimum gate-source isolation showed the necessity of a dielectric layer on the sidewalls of the source pillars. So, the samples are oxidized to form a 35 nm thick oxide on the Si-face and a 240 nm thick oxide on mesa-structure sidewalls. Note that, the thick oxide film grown on the sidewalls consumes unintentionally Al-doped source-finger-sidewalls and prevents

This metal coverage, on the edge and sidewalls, is believed to be one the reasons for the observed gate-source-leakage in our previous devices [8]. So, a new approach namely a salicide-like process has been included in our process. The salicide process is widely used in Si-technology for self-aligning purposes and involves the reaction of a thin transition metal film with

Figure 4. (a) and (b) SEM photos of the completed device. (c) Device cross-section schematic (Dark to light green: high to lower doping n- SiC, red: p- SiC, yellow: cyclotene, grey: SiO₂, light orange: Ni contact, dark orange: Au overlay).

formation of a leaky gate-source p⁺-n⁺ SiC junction. The horizontal oxide is removed subsequently by RIE.

silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes. However, in the

present case the salicide process has been used successfully for gate-source isolation purposes as the gate-source leakage has been greatly reduced.

The silicide process starts by a thermal annealing of Ni contacts at a temperature of 750°C. This anneal temperature is selected because it is enough for a nickel silicide phase formation between the Nickel/SiC physical contact, but it is not enough for a Nickel/SiO₂ reaction and there is an obvious distinction between “pure” Nickel and Nickel silicide. After that, a diluted standard SPM chemical solution (H₂SO₄:H₂O₂) is used to selectively remove the non-reacted Nickel metal from all the unwanted areas (pillar sidewalls and source pillar edges). Following, the device is annealed a second time at 1000°C leading to the best source-gate ohmic contact performance (Fig.3a).

A 100 nm thick Ni layer is also deposited on the wafer back side and then, the samples are annealed at 1000°C in vacuum to form ohmic contacts.

The morphology of the annealed front contacts is shown in Fig.3a.

The next process step is the application of a trench filling dielectric its curing and etching-back to expose the mesa-structure tops with source contacts. The usefulness of this step is two fold. First, to planarize the source pillar tops for interconnecting them by a metal deposition. Second, to avoid any short between the source and the gate. Polyimide and benzocyclobutene (BCB or simply cyclotene) have been tested as the dielectric for filling the gate trenches and in both cases a planarization and an etch back process are required. It has been found that the polyimide is not very suitable for planarization purposes while the BCB-cyclotene has excellent dielectric and planarization properties. The BCB film is deposited all-over the surface by spin coating and it is much thicker than the height of the source pillars. It is etched-back down to the source finger tops (Fig. 3b) with pure SF₆ reactive-ion-etching (RIE).

Figure 5. SEM micrograph of a short device cross-section.

The etching back of the BCB is happen in two steps. The planarization of the BCB with the source pillar tops is performed firstly. Then, a lithography is performed (the third lithography step) followed by the RIE etching to open the gate pad contacts (Fig. 3c).

Finally, a final fourth lithographic step was employed for depositing and patterning the common source and gate pad Ni/Au metal overlay (Fig. 4a&b). Edge termination is provided by a self-aligned multiple floating-guard-ring (GRs) structure (Fig.4c).

The cross-section of a fabricated TI-VJFET is shown in Fig. 5.

Devices with different channel widths (1.5, 2, 2.5, 3, 4 and 5 μ m) have been fabricated and allowed better understanding of transistors operation.

Figure 6. Experimental and simulated transfer characteristics for $V_{DS}=0.1V$ of the long channel device with 2μ m of channel width.

3. DEVICE MEASUREMENTS

On-wafer I-V measurements were performed with a Keithley 4200 parametric analyser up to 200V. On-state I-V characteristics were also performed in pulsed mode to avoid self-heating of the devices and the gate has been biased below its 2.7-V built-in potential value to maintain voltage-control capability (high I_D/I_G gain). Measurements at higher voltages have been performed with a Tektronix 370 curve tracer while the samples were covered with a liquid of high dielectric strength (Fluorinert[®]).

The measured characteristics were modeled with an analytical model and a finite element (TCAD) model. The analytical approach is based on typical semiconductor theory [9] for extracting output ON and transfer I-V as well as C-V characteristics, while a combination of previously published models [10] is involved for the simulation of forward blocking I-Vs. An iterative approach has been adopted to take into

account the voltage drop in the drain region and thus, connect extrinsic and intrinsic drain voltage. Both electric-field independent and dependent mobility models have been considered to evaluate their suitability for the JFET modelling. Finally, the model describes in a unified way the linear and saturation operating regions.

The TCAD SILVACO^c tool has been also employed for a finite element simulation. A simplified structure

Figure 6 shows typical experimental transfer I-V characteristic for the long devices. Both models agree on the value of the threshold voltage when taking into account the correct channel width, which often differs from the that of the mask due mainly to lateral straggling of the gate implantation. The long channel devices have a higher, in real value, threshold voltage as the lateral straggling reduces the effective channel width.

Figure 7. Pulsed measurements and simulated output characteristics of the long channel device with $3\mu\text{m}$ of channel width (right) and of the short channel device with again $3\mu\text{m}$ of channel width (left).

similar to that of the figure 1 has been simulated without taking into account edge termination and Gaussian tails of the implanted atoms space profiles. The default SILVACO values for material parameters have been used as a first approach before any refining to better describe experimental results.

Figure 7 shows the output ON I-V simulated and experimental characteristics for the two device types. The experimental curves correspond to pulsed measurements with long OFF times in order to approach isothermal measurements conditions. This allows to not consider device self-heating in the simulation models.

Figure 8. Experimental and simulated blocking characteristics of the long channel device with $1.5\mu\text{m}$ of channel width (left) and of the short channel device with again $1.5\mu\text{m}$ of channel width (right).

The shorter length device seems difficult to be correctly modelled with the analytical model as the drain-bias induced effect has to be taken into account even for the ON characteristics in order to correctly model the JFET operation. Long channel devices result in lower current densities due to higher R_{ON} values (around 6 and 12 $m\Omega \cdot cm^2$ for the short and long devices respectively).

The transistor blocking (Fig. 8) exhibits a triode shape, which is typical for a static-induction transistor operation. The short channel device presents very low blocking voltages (and corresponding voltage gain values <10) not exceeding 250 V (best case). The long channel devices exhibited blocking voltages up to 800V and voltage gain values up to 50. This difference between the two devices is expected from the SIT mode of operation [6]. Nevertheless, the breakdown voltage of the long channel devices is limited from the fact that the tops of the guard rings (Fig. 4) are highly doped.

course, this drop of the C_{OSS} value does not appear if we limit the graph in low V_{DS} values.

4. CONCLUSIONS

This paper presents the design consideration, fabrication and electrical characterization of 4H-SiC TI-VJFETs with different channel lengths and widths.

Generally speaking, the 4H-SiC TI-VJFETs are characterized by a rather simple process technology in comparison to the transistors like MOSFETs and BJTs. The major fabrication issues deal with the demanding lithography resolution and the isolation of the gate-source junction. The former has been addressed by a self-aligned approach offering in addition the advantage of a reduced number of photolithography steps. The latter has been addressed by incorporating in the process

Fig. 9: (a) C_{ISS} , C_{OSS} , C_{RSS} measurements at $f=1MHz$, (b) Blocking characteristics of the same short channel device.

In figure 9a, we can see the C_{ISS} , C_{OSS} , C_{RSS} from the short channel devices with the smallest channel width (1.5 μm nominal). The gate bias was equal to -15V, during the measurements with V_{DS} sweep, to ensure the off state of the device. All the curves exhibit a descending tense with the V_{DS} rise. The C_{OSS} decrease very abruptly reaching 0 at around $V_{DS}=30V$ and for higher bias values continue to negative capacitance values. Negative capacitance is usually a sign for strong inductive contributions to the impedance. Capacitive and inductive contributions are exclusive. You can only see one or the other, at least at fixed frequency. The increase of inductance can be explained from the fact that the channel becomes conductive above a V_{DS} value (SIT effect). Indeed, by looking the corresponding blocking I-V characteristic (Fig. 9b) the channel becomes conducting for this combination of V_{GS} and V_{DS} values. This conduction in the channel leads to negative values of C_{DS} and consequently of C_{OSS} . Of

a series of steps like a sidewall oxidation and a salicide-like approach for the Ni metallization on top of source fingers. The beneficial effect to the SiC surface, of a C-cap formation prior to post-implantation annealing has been demonstrated. Cyclotene seems to be more suitable for planarization and gate-to-source isolation purposes.

The electrical characteristics showed that the deeper gate transistors exhibit higher on-resistance values and lower leakage currents as expected. The blocking characteristics and consequently the rated voltage class are determined by a static induction effect and therefore rather from the channel geometry than from the drift layer doping and thickness. The advantage of the hereby proposed technology is its simplicity as only four photolithography steps have been employed for the edge termination of self-aligned guard rings.

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6. REFERENCES

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