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PROTOTYPING AND CHARACTERIZATION OF 1.2KV SIC SCHOTTKY DIODES FOR TWTA APPLICATION: THE CHALLENGE TO MEET THE USER SPECIFICATION

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1. INTRODUCTION

In Space applications the interests in SiC devices is growing due the benefits in terms of saving mass, increasing power, and for extreme environments (high temperature and high radiations levels).

Benefits based on the main features of SiC base material (high energy gap, high electric field breakdown in combination with reasonably high electron mobility and high thermal conductivity - 3 times higher than Si -) led to the following expected and in some cases already proven capabilities for power application: low on-state voltage (100 to 200 times lower on resistance x total gate charge with respect to Si), low leakage currents (order of magnitude lower than in Si devices), low recovery charge, fast turn-on and turn-off, high blocking voltage (> 2 KV), high power density [1-2]. Higher reliable operating junction temperature have been also demonstrated above 300°C [3-4].

The high thermal conductivity combined with the large band gap and high critical field provides SiC devices a great advantage. More specifically, the large bandgap and the breakdown field allow very thin and highly doped thicknesses in the stall region and therefore with very high conductivity. This implies that have the ability to switch high frequency power with less loss.

The EPC (Electronic Power Conditioning) for TWT (Travelling Wave Tube) is a converter that provides high voltage (up to about 8 kV) and average power (up to about 300W), and therefore is an application where SiC devices can be particularly attractive. An EPC feeds one or two traveling wave tubes, forming a high power transmitter. A telecommunications satellite can embark from a few tens to over 100 of these sets. Therefore any topological simplification and reduction of mass per set is essential. The EPC typically operate under a baseplate temperature about 65°C, however traveling wave tubes are exposed to baseplate temperatures around 95°C. Increased operating temperature for EPC, using SiC semiconductors, allow simplification of the satellite relative its thermal design, a reduction of the distance between the EPC and the TWT and therefore reduced size and mass, increased system reliability.

In the paper a summary of the technological issues encountered during the design of the SiC diode, in order to comply the optimized performances needed for the rectifier module in a next generation EPC for TWTA working at temperature higher than 65°C is reported. The static, switching and endurance electrical test characterization is specifically addressed.

The present study makes part of Work Plan of the Basic Technology Research Programme (TRP) funded by ESA falling in the category of Technology push for a new generation of space electronics units.

2. CRITICAL ANALYSYS

For the high voltage rectifier module, inside the EPC, the diodes should have the following specification to represent an improve respect to the silicon diodes use actually. Tab. 1 shows the SiC diodes requirements. Regarding the switching performances, the new diodes requires a near zero recovery current and near zero reverse recovery time, in comparative with the silicon ones.

Table 1.- Electrical SiC diodes requirements.

SiC Diodes parameter	Target specifications
$V_{breakdown}$	1200V goal 1500V
I_f max at T_{op} max (case) ≥150°C	2A
I_r max @ V_r =1300V	≤10uA@25ºC ≤50uA@130ºC
V_f @ 0.1A	≤0.95V @ 25ºC ≤0.70V@100ºC
I_{max} non repetitive surge	100A (t_{pulse}=10us)

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SiC Diodes parameter	Target specifications
current	
I_{max} repetitive surge current	30A
C_{in} @400V, 1MHz	<30 pF
Qc @400V, 1MHz	≤20nC @ 25ºC <30nC @ T_j max

The key parameter for the devices was the forward voltage drop at 0.1A and 100ºC. However, we also have to consider a low leakage current at 1200V (<10uA). We also have to deal with a low input capacitance and a short switching turn-off time. Both these last requirements need to minimize the Schottky diode area, which do not benefit the forward voltage drop and the surge current capability.

On top of this a specific hermetic package compatible with a 6 Lead Leadless Carrier Chip (6L-LCC) package need to be considered to avoid the requalification of the potting process of the HV section of EPC. Then, a compromise has to be found in the design.

For these specifications, we can consider two types of devices, a pure Schottky or a Junction Barrier Schottky diode [5]. The cross section of both devices is shown in Fig. 1. The difference is in the P+ rings included in the active part of the JBS. The ratio P/N between the width of the P+ ring (L_P) and the distance between P+ ring (L_N) is a key parameter in the design of the JBS.

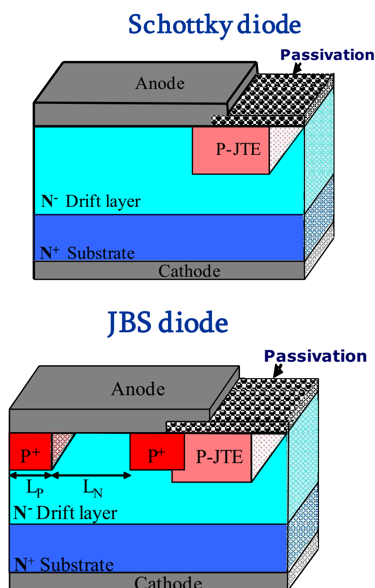

Figure 1: Schematic cross section of a Schottky diode and a JBS diode, including high voltage termination (JTE).

In the Tab. 2, we select the 3 main design/technology parameters, which will influence the trade-off between forward voltage drop, reverse leakage current and switching time.

We have designed JBS diodes with two Schottky barrier height and we have seen that with the high barrier configuration we do not fill the forward voltage specs, and that with the low barrier configuration, we do not fit the reverse current specifications. Ideally, we should then implement a Schottky contact with a barrier height between the two values. Unfortunately, this is not obvious as the usual metals used in Schottky contacts metallization in microelectronics have either lower barrier than (like Ti, W, Mo) or higher barrier (like Ni,, Al, Au). Even if we could find such metal, with non-usual Schottky metals, we have the risk to get a lot of stability and reliability problems. We have also tested different JBS Ln/Lp dimensions, showing some different distribution of the forward voltage drop versus the reverse leakage current.

Finally, compared with existing commercial technologies, we propose the following possible innovation and trade-off:

- JBS diodes for higher reliability and current peak capability.
- Use of W based Schottky metallization instead of Ti.
- Optimisation of the top metallization layer to increase current peak capability.
- Optimisation of the design of the Schottky metallization edge to withstand a maximum of transitory peak current
- Optimisation of the termination using the novel JTE + rings design to improve reliability
- Use of optimal starting material with last developments of EU supplier

Table 2.- Trade-off conditions

Design/technology parameter	Forward voltage	Reverse current	Switching time (C_{in})
Schottky barrier height increases (Schottky metal choice)	Increases	Decreases	Not sensitive
JBS instead of Schottky	Increases	Decreases	Increases (at high T^a)
Diode area increases	Decreases	Increases	Increases

The form factor required to meet the existing system board device footprint was the main driver for the design of the diode package. Using this as the main design rule for the package meant that the design dimensions were constrained to be compatible as a drop in replacement for a D5-B board footprint, similar to a standard 6 Lead Leadless Carrier Chip (6L-LCC) package. In order to accommodate the new die design, the standard 6L-LCC package had to be modified with the lead positions kept constant relative to the device centre line as per figure 2

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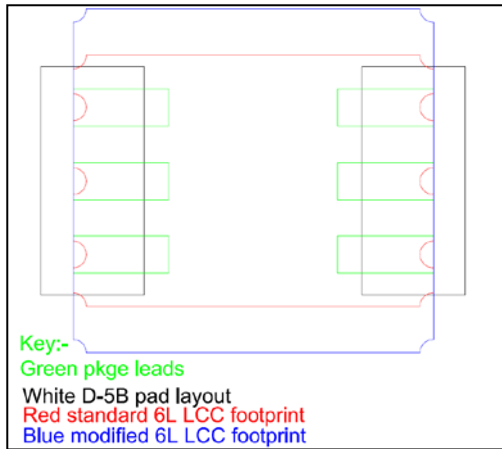

Figure 2: Drawing of the modified footprint compared to the standard D-5B and 6L LCC

A compromise in the package design between its thermal performance and form factor had to be made as the board footprint dictated the dimensions and lead positions for the new package. As a result, a bespoke thermally optimised packaged with a simulated thermal resistance in accordance with JEDEC standard JESD51-14 of under 2 °C / W was designed. Due to the constraints of the design, the compromise of the package lead positions meant that attaching a heat sink to enhance the thermal efficiency of the package when mounted onto the board is not possible. Further works on other designs that incorporate a built-in heat sink are currently being investigated.

3. STATIC ELECTRICAL CHARACTERIZATION

Steady-state electrical characterizations have been performed under a wide temperature range (-55ºC, 25ºC and 100ºC). The evolutions of two parameters, which may vary with temperature, have been monitored: forward voltage and reverse current. Tab. 3 resumes the measures done for 130 devices.

Table 3.- Experimental results of SiC diodes

Temperature	V_f @ 0.1A	I_r @ V_r =1300V
-55ºC	0.817 V	5.8 µA
25ºC	0.691 V	41.4 µA
100ºC	0.590 V	
130ºC		1262.6 µA

These parameters have been also measured in two flight existing Silicon diodes (Si-1 and Si-2) an in one commercial SiC diode (SiC) for comparison reasons. Fig. 3 and 4 shown the comparison of these parameters and its evolution with the temperature.

Regarding the voltage forward drop (Vfwd), at 25ºC, the best case is the SiC diode developed due to the optimisation process done. At 100ºC the worst case is the commercial SiC diode and the best is a silicon diode Si-1 very close to CNM SiC diode developed. The diodes fabricated met the requirements for Vfwd at both room and high temperature.

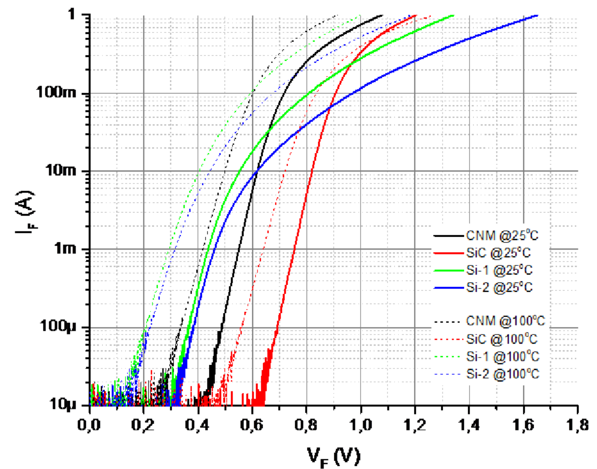

Figure 3.- Forward characteristic I-V

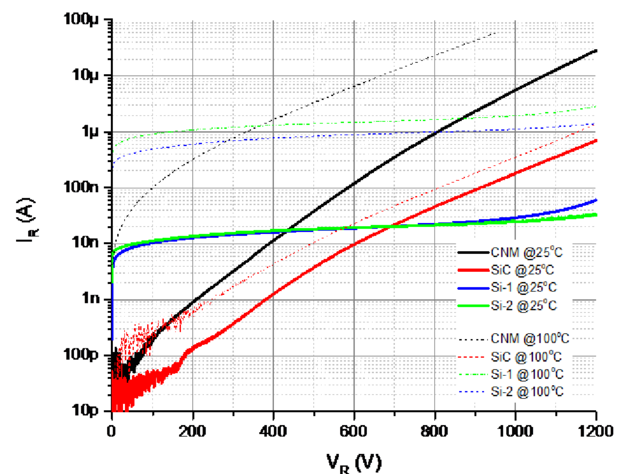

Figure 4.- Reverse characteristic I-V

The good behaviour in forward mode is not conserved to the reverse mode. The silicon diodes present a lower reverse current than the SiC diodes for higher blocking voltage. In Fig. 4 at 100ºC up to 300V the SiC diode developed is the best compared with the flight silicon diodes. By sorting the best diodes we can reduce the medium reverse leakage current. In this lot, we did obtained some diodes with reverse leakage current 3 to 4 times lower than the medium values reported in figure 4, with negligible difference in the forward characteristics. As a matter of facts, the starting material has a important effect on the reverse current. In this study e.g. one of the wafers showed 3 times lower leakage currents than the

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other two wafers.
Therefore a trade-off between the optimisation in the forward voltage drop and the reverse current characteristic will be chose.
As future development slight reduction of the diode area to better adjust the forward voltage drop to the 0.7V @0.1A @100ºC specified can be considered. This would also help gain on the input capacitance value to reach specs, together with a decrease of reverse current. On the other hand a smaller die could fit into packages with standard dimension and that offer a more effective heat sink performance.

Taking into account the application, high voltage module for EPC, one of the most important things is the risk for thermal runaway. The rectifiers are placed in a molded module together with the filtering capacitors, and it's mandatory maintain the temperature below a certain value. The thermal runaway is mainly due to the reverse recovery charge (Qrr) during the turn off process, without forgetting the contribution of the leakage current in lesser importance. Therefore we need to assure that the SiC diodes developed are temperature independent, to maintain the Qrr mainly constant.

4. SWITCHING CHARACTERIZATION

To extract switching characteristics of the SiC Diodes, we have designed a double pulse tester, specifically designed with a PCB layout and probes, taking attention to minimize the ringing effects on the measurement.

The following parameters have been measured during the OFF switching process for -55ºC, 25ºC and 175 ºC to characterize as a function of temperature. The turn-off conditions are V_{AK} = 900 V and I_F = 1.5 A:

- Maximum reverse recovery current (I_{RRM})
- Reverse recovery time (t_{rr})
- Reverse recovery charge (Q_{rr})
- Turn-off Energy (E_{off})

The next figures show box charts where has been analysed the temperature dependence of each parameter in function of the switching speed. The boxes contain all devices data for a specific di/dt and temperature. The width and height of the box provide information of key values from summary statistics. The box is determined by the 25th and 75th percentiles and the whiskers are determined by the 5th and 95th percentiles.

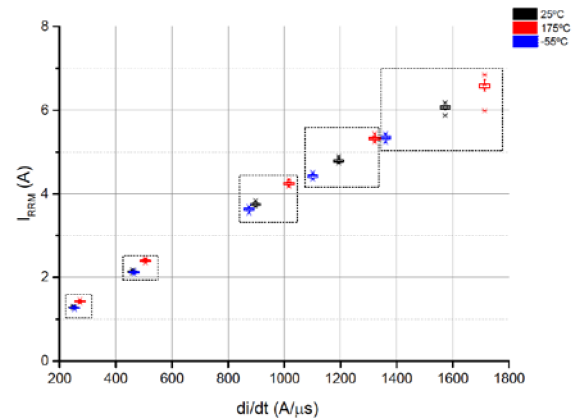

Figure 5.- I_{RRM} temperature and di/dt dependence.

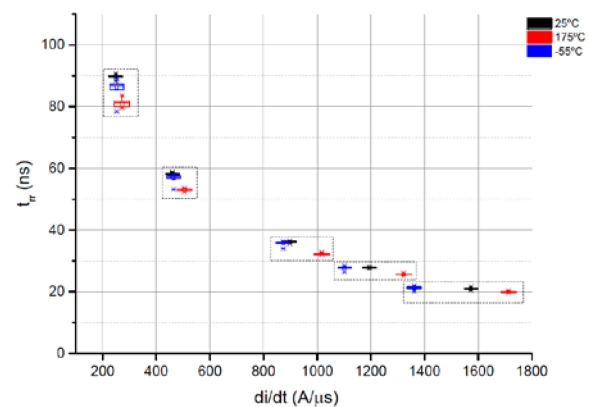

Figure 6.- t_{rr} temperature and di/dt dependence.

For a constant temperature, the reverse recovery time (t_{rr}) decreases with di/dt, representing good switching performances for high frequency applications, although I_{RRM} increases, the energy loss (E_{OFF}) associated with the turn-off is less when it is switched faster.

Regarding the switching behaviour respect to the temperature, when temperature increases the diode switching process is faster, increasing the di/dt, while the t_{rr} and the I_{RRM} are nearly temperature independent. Only a small variation with the temperature is shown to a lower di/dt, where I_{RRM} increase with the temperature and t_{rr} decrease slightly.

At room temperature we have done the switching characterization for the Silicon diodes and for the commercial SiC diode, to compare with the develop SiC diode. Fig. 7 and 8 shows the experimental results.

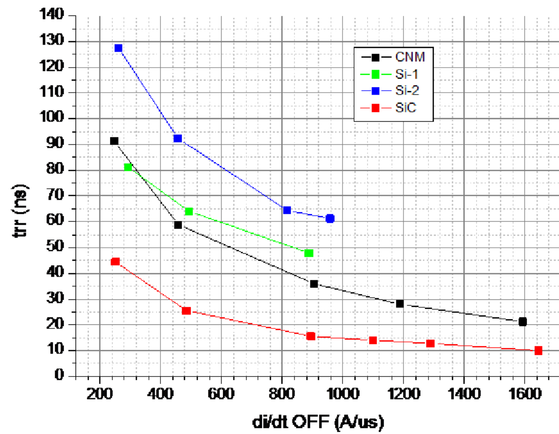

Figure 7. t_{rr} *diodes comparison*
(RT, V_{AK} = 900 V and I_F = 1.5 A)

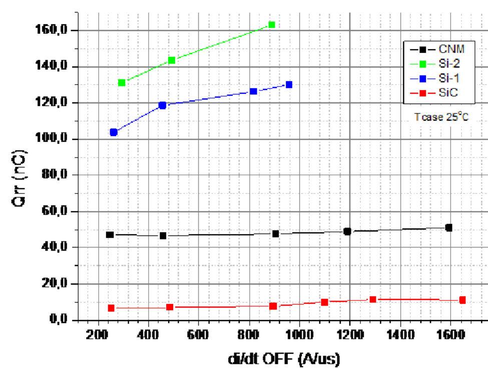

Figure 8.- Q_{RR} diodes comparison
(RT, V_{AK} = 900 V and I_F = 1.5 A)

5. DESTRUCTIVE CHARACTERIZATION

Destructive tests were performed according the relevant test procedures. Indeed, specific screening methods and qualification methodologies have to be defined for SiC devices. In reference [3] we proposed and reported a specific characterisation procedure for SiC high temperature diodes. We have done a test campaign for the developed SiC diodes to obtain the absolute maximum currents ratings, repetitive and non-repetitive, and a power cycle test in order to determine the conditions that the diode is able to support more than 2000 power cycles without any detrimental effect.

5.1.- Absolute current ratings.

Four devices have been tested to obtain the maximum absolute current rates. Tab. 4 shows the experimental results.

Table 4.- Experimental results absolute current rate

	Maximum Current (A)	Test conditions
I_{FSM} (A)	415	t $_{PULSE}$: 10 µs - Tcase: 25 ºC
I_{FRM} (A)	215	Nº of pulses: 5 - Tcase: 150 ºC t $_{PULSE}$: 50 µs, Duty 0.5%

Due to the higher die size used compared to commercial devices, we obtain a high surge capability. In order to optimise the overall parameters, if the application doesn't need a higher surge current, we can reduce that, reducing the die size and also a leakage currents reduction will be obtained.

5.2 Power Cycle Test.

The Power cycling test is an accelerated lifetime test, to verify the ability of the 1.2kV SiC Diodes under development, to sustain repeated thermo-electrical stresses. An active Power Cycling of constant timing (ton=const. and toff=const.) based in a load current conducted through the SiC diode, which is heated by its internal losses generating a temperature gradient, has been tested. When the desired junction temperature is reached, the load current is switched off. We placed the DUT on a heat sink, without forced cooling, and a natural conducted and radiation-cooling phase concludes the cycle. The heat sink temperature is relatively stable, while the junction of the DUT experiences sharp temperature fluctuations.

The Power Cycle test conditions are:

- $\Delta T_C \simeq$ 40ºC, $I_{F\ PULSE}$ = 4 A
- t_{on} = 5 sec , t_{off} = 30 sec.
- $T_{(case_min)}$= starts at 110ºC.
- If $T_{(case)}$=200ºC the test shall be stopped.

Considering the robustness, the results of power cycle test shown that the SiC diodes developed can withstand more than 2000 cycles if the case temperature swing is less than 40ºC, with a small increase (less than 5%) in the forward voltage at 0.1A. In Fig. 9 the evolution of the forward voltage rising up to 8000 cycles in the worst case for a ΔT_C of 40ºC is shown.

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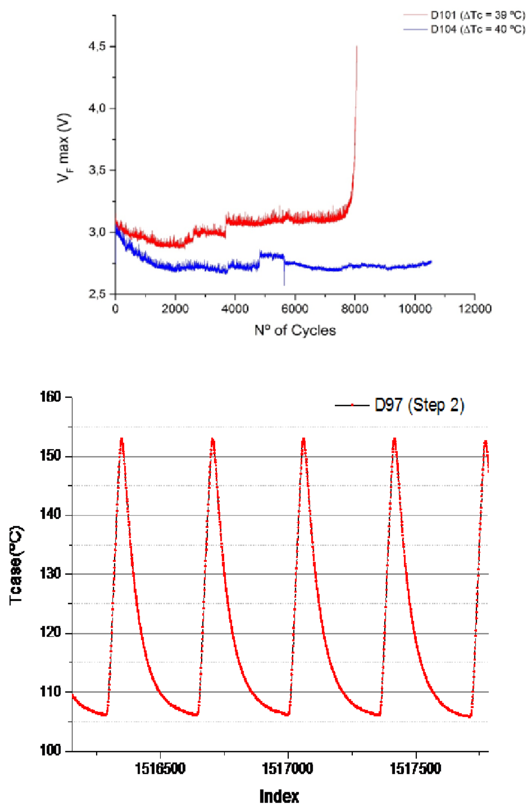

Figure 9.- $V_{F\ (max)}$ vs. nº of cycles (ΔT_C = 40 ºC range)

5.3 Specific Screening requirements

Schottky Barrier Stabilization: Drift in the barrier height leading to a Vfwd increase of 1.5% and a decrease of the leakage current, was observed for devices biased with maximum nominal currents (2 amps) for some time. This drift stabilizes after a given number of hours of stress. Diode full stabilization time depends on the current applied and seems to also depend on the sample. Screening of these diodes shall include a stabilization test in order to ensure a stable final diode. Fig10 shows almost full stabilization after 1 hour with Ifwd = 2 A at 25ºC.

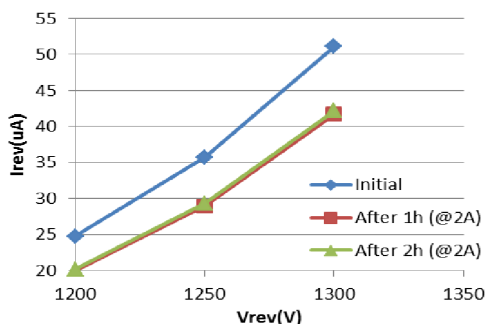

Figure 10.- Drift in Irev at HV after stabilization

Latent defects detection at low temperature: some defects that could lead to early failure of the component arise only while measuring the devices at low temperature like shown in fig 11. Also some failures are observed in a reverse measurement at room temperature after the low temperature characterization. Screening of these devices must always include this test sequence in order to detect and screen out this small population of devices.

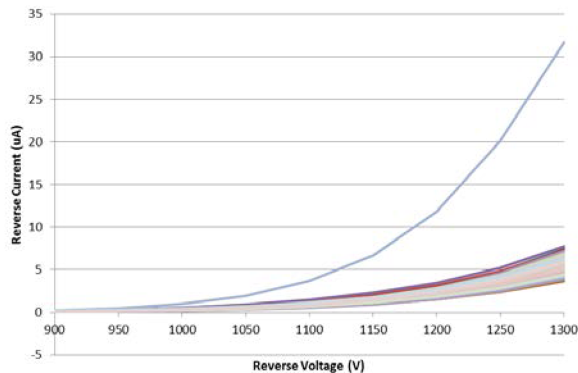

Figure 11.- Out of family behaviour of a diode (-55ºC, 128 devices in the graph)

5.4 Endurance test results

Prior to endurance tests, power step stress tests were performed identifying the limits of the device. Temperature step stress arise drift in characteristics for storage temperatures of 200ºC and higher because of package degradation. Power step stress test arise different, again package driven, limitations. The SMD solution fitting the final application limited the forward current for all the long lasting tests to 2 amps.

Endurance tests were performed obtaining good results in both reverse (fig. 12) and forward (fig. 13) mode after a thousand hours. In this last figure can be seen that stabilization of the barrier was not achieved in only two hours of sample preparation at 25ºC but it is also clear that no degradation occurred since no changes were observed during the last 267 hours of test.

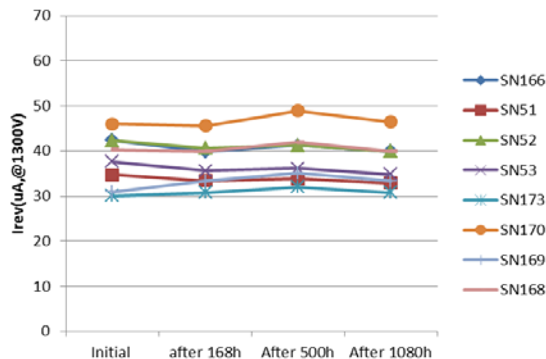

Figure 12.- HTRB (1080h, 100ºC, Vrev=1020V) intermediate reverse characterization at 25ºC

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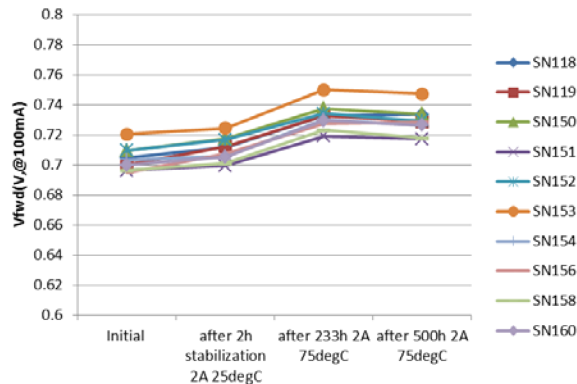

Figure 13.- Accelerated Elec. Endurance (Subset 2, 500h, 75ºC, Ifwd=2A) intermediate reverse characterization at 25ºC

5.5 Heavy ions test campaign

Based on the experience gathered on previous studies conducted by ESA, an heavy ions test campaign has been performed with the objective to characterise better the already known and shown in many paper and publication SEE sensitivity of SiC Schottky diodes. Fifteen samples were tested in different beam conditions; an analysis of flux dependence has been also performed as well as verification of different annealing methodology.

The damages induced by ions are cumulative and depends on LET of the ions and on the electrical field across the junction. A general very limited Safe Operating Area of Vr ≤ 250V has been confirmed at LET=32.4 MeV cm^2/mg.

A linear degradation of the reverse current (Irev), directly proportional to the fluence of ions heating the junction has been observed. It is not therefore a standard catastrophic failure induced by a single particle but more an accumulation of defects in the active area (metal-SiC interface or in the epi-layer).

The damages are permanent and are affecting only the reverse characteristic. The barrier height is not affected. See fig 14 were an example of the degradation in reverse with a LET=32.4MeV cm^2/mg has been reported.

We have observed a partial recovery of the Irev characteristic after 16 hours of annealing at 200°C. This partial annealing has been considered curing interfaces states induced by ion exposure. However crystal defects in the epilayer seems to play an important role as well and cannot be recovered by the performed high temperature annealing.

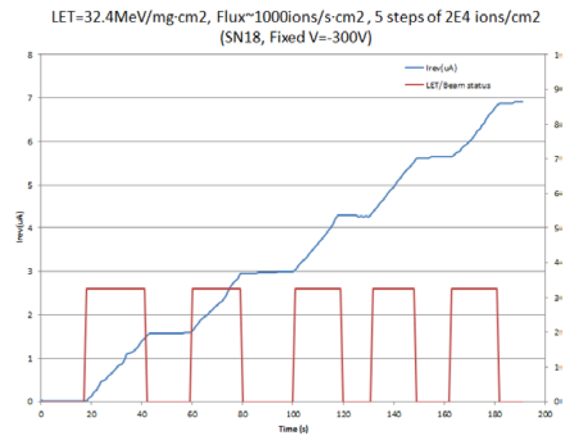

Figure 14.- degradation in situ of the Irev with a LET=32.4MeV cm^2/mg, comparison of Irev characteristic before and after the beam exposure

6. CONCLUSIONS

Different strengths are identified for SiC power devices, among them; high voltage operation seems the most promising in space applications. In the paper the development of an optimized design for a SiC diode able of improving the thermal and forward voltage drop performances of silicon diodes, used as high voltage diodes rectifiers, has been reported.

Samples of the diodes have been sent to potential user for validation in their test bench. They confirmed that the developed diodes meet and exceed the performances they were requiring for prototyping the next generation of EPC. In a second generation, improvement in the reverse current characteristics can be expected by some minor technology adjustments, which would not affect the rest of the characteristics.

Independently of the improvements of SiC semiconductors in the high voltage niche, another challenge is to enable major advances in Electric Propulsion (EP) in-space operations and transportation. Their very good performances in high switching frequency resulted in converter size reduction and improved dynamic response, which are key aspects for increasing system power density.

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The Power Processing Unit (PPU) is a technically challenging and expensive part of each EP system (up to 50 % of the cost-indicative). Power key performance beyond state-of-the-art may indeed be more challenging on the PPU side than for the thruster. Also for telecommunication applications dual mode EP systems are required, which can switch between a high thrust and lower thrust mode for station keeping.

The high sensitivity to heavy ions has been confirmed to be the major drawback of SiC Schottky technology for space application. It has been confirmed that heavy ions induce a cumulative degradation of reverse current and no a real sudden catastrophic effect. The concept of derating down to a demonstrated safe operating area seems at the moment the more promising choice to mitigate the heavy ions sensitivity taking advantage of the high blocking capability of SiC.

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