LOW SIDE GAN FET DRIVER FOR SPACE APPLICATIONS

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ABSTRACT

This paper reports the results of preliminary single event effects (SEE) testing of the Intersil ISL70040SEH, a single low side driver specifically designed to drive enhancement mode power GaN FETs.

1. Introduction

Recently, wide band gap semiconductor devices such as GaN and SiC have been gaining interest in power management for space applications. These devices feature higher breakdown voltage, lower $R_{DS(ON)}$, and very low gate charge enabling power management systems to operate at higher switching frequencies while still achieving higher efficiency and a small solution footprint. There is an added benefit, especially from GaN devices, that make these attractive to the space market. Studies have shown that these devices are inherently radiation hard to total ionizing dose. However, GaN power transistors have a limited gate to source voltage range and with that comes the complexities of providing the right grate dive, a low inductive path and the correct timing. In this paper we report results of destructive and non-destructive SEE testing of the ISL70040SEH, a low side GaN FET driver designed for space applications, together with a brief discussion of the part's electrical specifications and how the device solves many of the problems associated with using GaN FETs in power management space applications.

2. The ISL70040SEH Low Side Driver

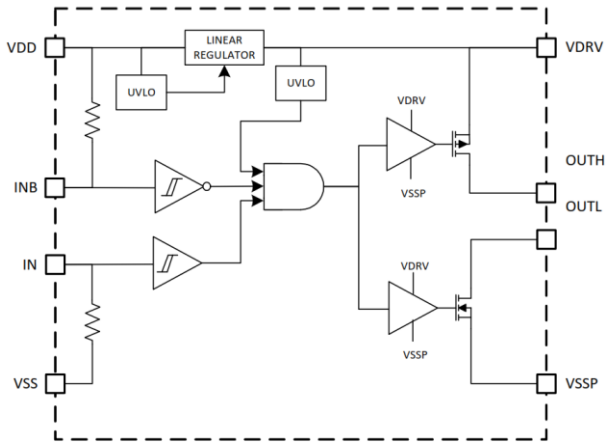

Figure 1. ISL70040SEH block diagram

The ISL70040SEH is a low side driver designed to drive enhancement mode Gallium Nitride (eGaN) FETs in isolated topologies, boost type configurations and synchronous rectification. The ISL70040SEH offers both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive in a single device type (refer to Fig. 1).

Inputs of the ISL70040SEH can withstand the input voltages up to 14.7V regardless of the VDD voltage. This allows inputs of the ISL70040SEH to be connected directly to most radiation hardened PWM controllers. The split outputs of the ISL70040SEH offer flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance in either the turn-on path and/or the turn-off path. The nominal operating supply voltage range is 5V to 12V and includes an internal 4.5V series regulator with an under-voltage lockout (UVLO) circuit. When the voltage is below the UVLO threshold, the IN and INB are ignored and an internal pull down device keeps the GaN FET off.

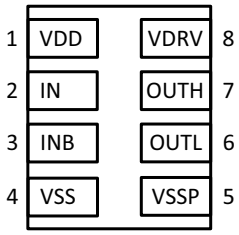

Figure 2. ISL700040SEH pin configuration.

The ISL70040SEH operates over the military temperature range from -55°C to +125°C and is offered in a 8 pin hermetically sealed 6mm x 6mm ceramic leadless chip carrier (CLCC) package. The package was designed to reduce parasitic inductance to mitigate the risk of excessive overshoot when driving the gate of the GaN FET. See Fig. 2 and Tab. 1 for pin configuration and pin description.

The ISL70040SEH is targeting a total dose (TID) rating of 100krad(Si) at a high dose rate (50-300rad(Si)/s) , 75krad(Si) at a low dose rate (< 0.01rad(Si)/s) and will be acceptance tested on a wafer by wafer basis. The ISL70040SEH is also SEE rated for both destructive and non-destructive effects to a linear energy transfer (LET) value of 86MeV·cm^2/mg. Single-event transient (SET) response has emerged as a key issue in power management parts, and this paper will concentrate on ISL70040SEH SEE results.

Table 1. ISL700040SEH pin description.

Pin Name	Description
VDD	This is the supply for the internal linear regulator of the ISL70040SEH.
IN	Non-inverting inputs pin with controls OUTH and OUTL outputs.
INB	Inverting inputs pin with controls OUTH and OUTL outputs.
VSS	Supply ground. Connect this pin to VSSP via the PCB ground plane.
VSSP	Power supply ground, Connect this pin to VSS via the PCB ground plane.
OUTL	The output low pin is the gate driver turn-off output.
OUTH	The output high pin is the gate driver turn-on output.
VDRV	This pin is the output of the internal linear regulator and the gate drive voltage.

3. Performance of the ISL70040SEH

GaN FET devices have special gate drive requirements that must be considered when choosing the correct driver. Typically enhancement mode GaN FETs have a lower rated maximum gate voltage compared to silicon MOSFETs. Therefore, the driver should have a well-regulated gate drive voltage that is high enough to fully turn-on the GaN FET but low enough that it does not damage the gate of the transistor. The driver should also have high source and sink current capability to fully utilize the high switching speed capability of GaN devices. Inversely, high current drive capability also means low pull-up and pull-down resistance output stages. A low resistance turn-off path is essential to mitigate Miller turn-on. Lastly, sometimes the fast turn-on capability can lead to loss of efficiency due to overshoots or increase in EMI. In these cases it is required to slow down the turn-on of the GaN device. This is typically this is achieved with a diode and a parallel resistor series with driver output stage. However, this is not recommended due the low threshold of the GaN device and diode forward voltage drop. A driver with a split output stage allows to tune the turn-on and the turn-off speed without under driving the gate.

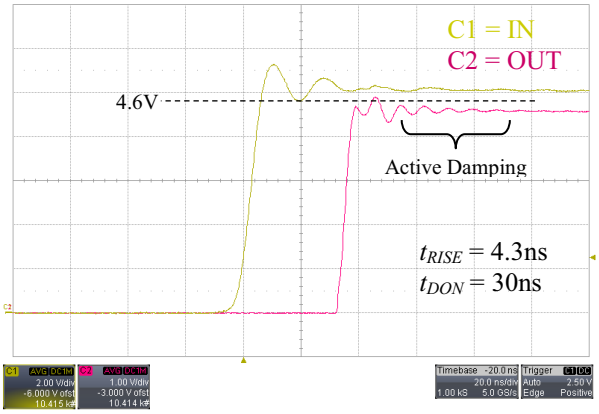

Figure 3. ISL70040SEH typical rising waveform

On the ISL70004SEH the gate drive voltage on the VDRV pin is regulated by the internal linear regulator to 4.5V. This tightly regulated gate voltage is high enough to fully turn-on enhancement mode GaN FETs but low enough to allow some overshoot, alleviating some of the complications of PCB design. The ISL70004SEH also has active damping output stages which changes the output impedance of the pull-up and pull-down paths to dampen overshoot and prevent the gate voltage from exceeding the maximum gate-source rating of enhancement mode GaN FETs.

Fig. 3 shows a typical rising waveform of the ISL70040SEH with a load capacitance of 1000pF and the VDD supply voltage at 12V. The input signal is on channel 1 (C1) and the driver output is on channel 2 (C2). Some of the key performance highlights are:

1. Gate drive voltage steadies to 4.5V with a peak of approximately 4.6V.
2. The rise time for 10% to 90% is 4.3ns.
3. The turn-on delay is 30ns. Some of the delay is due to the internal SET mitigation circuitry.
4. The dampen response of the output due to increased impedance of the output stage.

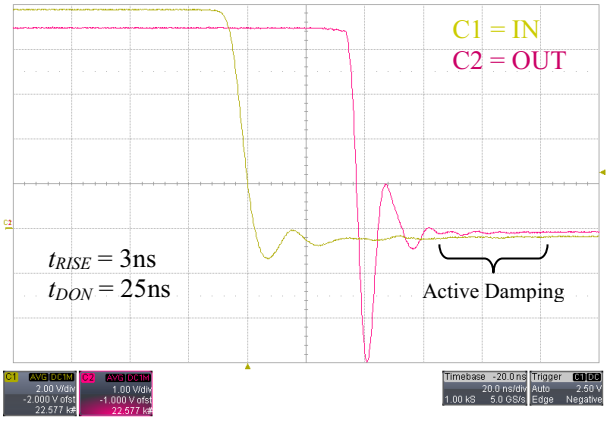

Figure 4. ISL70040SEH typical falling waveform

Fig. 4 shows a typical rising waveform of the ISL70040SEH with a load capacitance of 1000pF and the VDD supply voltage at 12V. The input signal is on channel 1 (C1) and the driver output is on channel 2 (C2). Some of the key performance highlights are:

1. The fall time for 90% to 10% is 3ns.
2. The turn-off delay is 25ns. Some of the delay is due to the internal SET mitigation circuitry.
3. The dampen response of the output due to increased impedance of the output stage.
4. Under shoot peaks at -3V, due to the strong pull-down capability. To minimize undershoot one may add an external resistor on the OUTL pin. The added impedance will also slow down the fall time.

4. SEE Testing of the ISL70040SEH

SEE testing of the ISL700040 took place at the end of August, 2016 at Texas A&M University (TAMU) cyclotron facility. Single event effects characterization was performed to determine its susceptibility to destructive effects including single-event latchup (SEL), single-event burnout (SEB) and single-event gate rupture (SEGR), and to non-destructive effects including single-event transient (SET).

4.1. Destructive SEE testing of the ISL70040SEH

During destructive SEE testing the ISL70040SEH was in an active configuration driving a 10nF capacitance load with a supply voltage on the VDD pin of 14.7V.

The device under test (DUT) was mounted in the beam line and irradiated with heavy ions of the appropriate species. The parts were assembled in 8 lead ceramic leadless packages with the metal lid removed for beam exposure. The beam was directed onto the exposed die and the beam flux, beam fluence, and select voltages and current in the device pins were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected via cable to the DUT. The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters, while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE displayed by the part. Events were captured by triggering on changes in the output. Tab. 2 summarizes the test conditions during heavy ion radiation for the destructive test.

Table 2. ISL700040SEH destructive SEE test conditions

Specification	Condition
VDD (V)	14.7
T_{CASE} (°C)	125
Species & Angle	Gold (Au) ions at normal incidence
LET	86MeV•cm^2/mg
Flux (cm^{-2}s^{-1})	5.00 x 10^4
Fluence (cm^{-2})	1.00 x 10^7
IN(V) & Frequency	0-10V square wave at 500kHz
INB (V)	0
C_{OUT} (nF)	10

The schematic of the test board is given in Fig. 5.

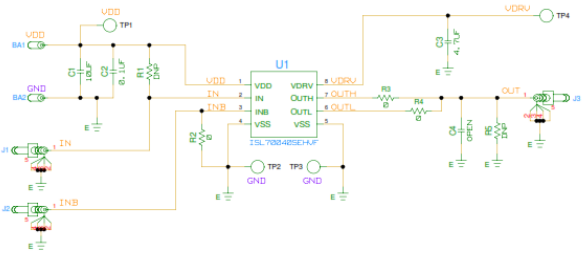

Figure 5. ISL70040SEH SEE test schematic

The supply current, input pin (IN) current and gate output voltage were monitored pre and post heavy ion irradiation. If any of those monitored specifications changed more than the specified criteria the device was considered a failed unit. Tab. 3 summarizes the specifications, conditions and the failure criteria used during destructive SEE testing.

Table 3. Destructive SEE testing failure criteria

Specification	Condition	Failure Criteria
I_{DD} Operating	F_{SW} = 500kHz	5% delta
I_{IN}	V_{IN} = 0V	50% delta
I_{IN}	V_{IN} = 13.2V	50% delta
Static I_{DD}	V_{IN} = 1.35V	5% delta
Static V_{OUT} LO	V_{IN} = 1.35V	50mV delta
Static I_{DD}	V_{IN} = 2.00V	5% delta
Static V_{OUT} HI	V_{IN} = 2.00V	50mV delta

Destructive testing results indicated no failures of the ISL70040SEH for a supply voltage of 14.7V at an LET of 86MeV•cm^2/mg. The final DUT was retested with a VDD supply of 15.1V. That DUT exhibited an increase in operating supply current larger than 5% and was considered a failure. Tab. 4 summarizes the results of destructive SEE testing.

4.2. SET testing of the ISL70040SEH

Single event transient tested utilized the same schematic as shown in Fig. 5. Both static and dynamic tests were conducted to characterize the SET behavior of the ISL70040SEH.

During the static test the driver was supply voltage was 4.5V and 13.2V, the min and max recommended operating range. The outputs were set in a high or low condition and a digital oscilloscope connected to the output was used to trigger on deviations greater than ±500mV. There was no capacitive load connected to output.

For dynamic testing the supply voltage was 4.5V and 13.2V. The input was driven with 0-5V square wave at 500kHz. A digital oscilloscope was connected to the output and use to trigger on a SET event that led to change of pulse width greater than ±50ns. There was no capacitive load connected to output.

Table 4. ISL700040SEH destructive SEE test summary

		IDD @ 10nF & IN = 500kHz, 0-xxV		IIN @ IN =0V		IIN @ IN =13.2V		IDD @ IN =1.35V		VOUT @ IN = 1.35V		IDD @ IN = 2.00V		VOUT @ IN = 2.00V		SEB
Device	Run	Pre (mA)	Post (mA)	Pre (nA)	Post (nA)	Pre (uA)	Post (uA)	Pre (mA)	Post (mA)	Pre (V)	Post (V)	Pre (mA)	Post (mA)	Pre (V)	Post (V)	
1	508	31.34	31.40	25	20	63	63	2.53	2.53	62u	61u	10.69	10.67	4.55	4.55	Pass
2	509	32.12	32.10	20	13	62	62	2.53	2.53	85u	82u	10.67	10.71	4.58	4.56	Pass
3	510	31.20	31.26	7	4	62	61	2.47	2.46	69u	69u	10.68	10.67	4.57	4.57	Pass
4	511	31.87	31.92	170	190	64	64	2.54	2.54	59u	64u	10.66	10.67	4.57	4.57	Pass
4	512	34.15	31.93	630	640	65	63	2.56	2.56	58u	59.00	10.68	10.71	4.57	4.58	Fail

Tab. 5 summarizes the test conditions for the static test in both the low and high states. Four devices were subjected to the test and no triggers were captured with oscilloscope. The ISL70040SEH is SET immune in the static condition. This is a very positive results as in a typical applications the driver will not unintentionally turn-on or turn-off the device and the output state solely relies on the input condition.

Table 5. Static SET test conditions

Test #	VDD	IN	INB	OUT	SET Trigger
1	4.5V	1.35V	0V	LO	0V ± 500mV
2	4.5V	2	0V	HI	4.5V ± 500mV
3	13.2V	1.35V	0V	LO	0V ± 500mV
4	13.2V	2	0V	HI	4.5V ± 500mV

Tab. 6 summarized the test condition for the dynamic test. Four devices were tested utilizing both conditions. There were no triggers captured on oscilloscope. This indicates the pulse width of the controller does not change more than 50ns. For test condition of 500kHz with 50% duty cycle, 50ns translates to 5% of the ON time of the pulse. If the switching frequency is increased to 1MHz for example with a 50% duty cycle a 50ns change means a 10% change of the desired pulse width.

Table 6. Dynamic SET test conditions

Test #	VDD	IN	INB	SET Trigger
1	4.5V	0-5V @ 500kHz	0V	PW ± 50ns
2	13.2V	0-5V @ 500kHz	0V	PW ± 50ns

5. Summary

The ISL70040SEH is radiation hardened low side GaN FET driver which contains all the features necessary to drive enhancement mode GaN FETs in space applications. The single event effect testing demonstrating no SEB or SEL with a supply voltage of upto 14.7V at an LET of 86MeV•cm^2/mg.

Single event characterization demonstrated that in a static condition the output does not change states with regards to the input condition. This means the device is SET immune and will not inadvertently turn-on or turn-off the GaN power transistor due to a heavy ion strike. Dynamic characterization results demonstrate that the output pulse width will not change more than 50ns. For low switching frequency applications 500kHz an below that is less than 5% change of a 50% duty cycle pulse width. As the switching frequency in increased the percentage is much larger and may cause and issue. Follow up SET characterization is planned for next year and the pulse width trigger may be reduced to 20ns or lower detect the minimum change in pulse width due to an ion strike.

6. References

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