MULTI-OUTPUT POWER CONVERTER, OPERATED FROM A REGULATED INPUT BUS, FOR THE SIREUS RATE SENSOR

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ABSTRACT

This paper describes a DC to DC converter designed to meet the power supply requirements of the SiREUS Coarse Rate Sensor (CRS) which is a 3-axis MEMS Rate Sensor (MRS) that uses a resonating ring gyro and will be used in different ESA missions. The converter supplies +5V, -5V, 3.3V, 1.8V and 40V and it has been designed and prototyped by Clyde Space Ltd with the EQM and FM units being manufactured by Selex ES. The first model was designed for a 28V un-regulated bus and the second model presented here has been designed for a 50V regulated bus. PWM voltage regulation was not used because of the noise requirements and the regulated input bus allowed an unregulated power stage approach. There are also stringent volume and interface constraints, which also affected the design. For such reasons, a fixed duty-cycle, quasi-resonant single-ended topology with output linear regulators has been implemented; having the advantages of providing low switching losses, low radiated and conducted noise and no over-voltage failure mode. This paper highlights the techniques used to satisfy stringent noise and protection requirements of the load.

1. INTRODUCTION

The CRS is a 3.6W (maximum) 3-axis rate sensor that is used continuously from just after launch to de-spin the spacecraft, until full ADCS stabilization is achieved. Thereafter it is used in standby (active or redundant) for fault detection isolation and recovery. The operational life is the same as the spacecraft mission and the radiation requirements are commensurate with that. On the ESA Sentinel-3 the gyros will be used for identifying satellite motion and also to place it into a pre-set altitude in association with optical sensors after its separation from the launcher, for Sun and Earth acquisition.

Many types of gyros have traditionally been two unit solutions with different (mechanical, thermal and electrical) interfacing characteristics for each unit which resulted in long interconnects and EMC/EMI issues. The CRS presents a more compact single unit, which is more attractive in traditional satellite applications as well as within the increasing range of small-micro satellites [1]. The PSU (Power Supply Unit) for the CRS must therefore follow the low mass and low volume requirements imposed by the design of the sensor. The PSU shall fit in a 75x75mm PCB.

Inside the MRS, a drive signal is applied to the detector drive plates at a nominal 14 kHz, which excites the silicon ring into oscillation [2]. Because the MRS is very sensitive to 14 kHz signals, a design requirement to minimize noise at that frequency, and also at the third harmonic, has been imposed. Filtering such low frequencies requires relatively large input filter components which has a major impact on the physical implementation of the PSU. The topology selected uses quasi-resonant switching to reduce the amount of high frequency noise generated in the system.

The use of Rad-Hard linear regulator integrated circuits has been considered in order to provide a compact solution to meet the regulation requirements of three of the five converter outputs within the volume constraints. The proposed IC is the ITAR free RHFL4913 from STMicroelectronics. This, however, for the 1.8V output, presented a problem in a previous implementation of the PSU for the CRS. The load for the 1.8V output is 800mW and the minimum input voltage of the RHFL4913 is 3V. This produced a 530mW hotspot on the PCB, which in turn, produced thermal issues in the CRS unit. A low-dropout linear regulator has been designed using discrete components to reduce the power dissipation of this output regulator. A very fast current protection has been implemented on this 1.8V series regulator to protect the load, which is an FPGA, from Single Event Effects (SEE).

2. ARCHITECTURE

Because of the limited volume allocated, the only PWM converter at first considered possible to fit the size of PCB was the simple Flyback converter because the inductor and transformer action required for PWM operation are all self-contained in a single Flyback magnetic component. But this was discarded for the

following reasons:

- The Flyback produces relatively high radiated and conducted noise due to its high peak switching current and voltages.
- PWM operation also produces variation in the magnitude of the harmonics and therefore of the magnitude of the noise.
- In the event of an SEE that keeps the Power MOSFET on for several cycles, the stored energy in the Flyback inductor will be high. When at the end of the SEE event the MOSFET turns -off, this energy is difficult to control in order to avoid an output-over voltage. Detection of an over-voltage fault is also difficult because during the time the MOSFET is on it is not possible for the over-voltage protection at the output to detect the fault. It can only detect over-voltage when the output begins to rise but at that instant the energy in the inductor has been already released. The only solution is to use a high power crow-bar across one or more of the output voltages. This solution is not favoured because it can lead to more complex failure modes.

The architecture selected is shown in Fig. 1. There is a common-mode filter followed by a damped PI filter. These two filters have been designed to provide 30dB of attenuation of conducted noise at the 14 kHz critical frequency. An LCL is used immediately after the filter to protect the converter against over-current due to an SEE produced in the converter circuits. This allows the converter to recover without damage from an SEE. Because the load of the LCL is inductive (i.e. the primary winding of the main transformer), feedback compensation of the LCL was required [3], [4], [5].
The requirement for the outputs to be isolated is satisfied by the single-ended transformer based topology. Each of the converter outputs has linear regulators to provide fine regulation and load current limitation.

2.1 Single-Ended Transformer Based Topology

Since the converter operates from satellite main bus, which is regulated from 46V to 51V, PWM regulation is not required. In addition, a single- ended topology using a single power MOSFET and voltage transformer has been selected. The MOSFET operates at a fixed pulse-width to give output voltages that follow the regulated input voltage. The fine regulation of the outputs is implemented by linear regulators, which also have the advantage of output noise suppression. This set-up gives a simple low component count solution to satisfy the size constraints of the PSU. Without PWM control, over-voltage failure mode is not possible. For example, if, the pulse–width changes due to a SEE, the output voltages will not change,
This topology does not require an inductor for its power stage. This frees up room for the relatively large (1mH) input filter inductor needed to provide the required level of attenuation of 30db at the 14 kHz critical frequency.
There is a start-up circuit that regulates the voltage of the control electronics to 14V thus allowing the PSU to start-up upon power-on. The main converter has an auxiliary winding in the main transformer that provides 15V on the auxiliary supply voltage and "backs-off" the operation of the more inefficient start-up regulator.
An under-voltage detection circuit switches the converter off when the voltage on the main satellite bus goes below 46V, and on again at 47V.

2.2 Quasi-Resonant Conversion

With normal square-wave operation the voltage at the drain of the main switching MOSFET, $M_{SW,}$ will increase to values higher than twice the input voltage as it is explained in the following paragraphs. With a 50V input voltage, the voltage at the end of the "off" time will be in the region of 130 to 150 volts. At turn-on, M_{SW} switches from this high voltage to zero in few nano-seconds. This produces a very high *dv(t)/dt* which, in turn, causes high frequency radiated noise. This noise is capacitively coupled to the input and outputs causing EMC problems. In order to minimize the amount of radiated noise generated in the power converter, quasi-resonant switching conversion has been implemented. The magnetising inductance resonates with the output

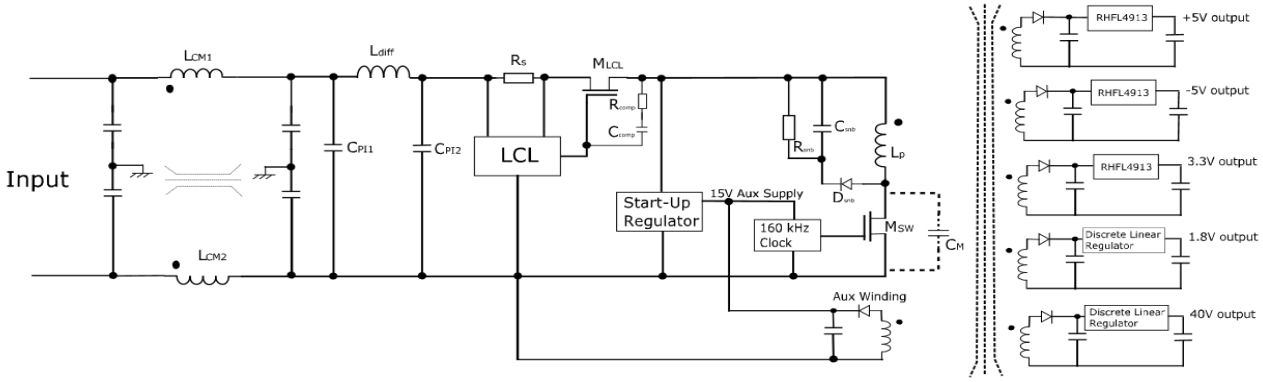

Figure 1. PSU Architecture

capacitance, C_M, of M_{SW}. Assuming a fix value of C_M, the voltage waveform on the drain during the "off" time is dictated by Eq. 1.

$$v(t) = V_{IN} + I_{L_p} \cdot \sqrt{\frac{L_p}{C_M}} \cdot \sin(\omega_o t) - V_{IN} \cdot \cos(\omega_o t) \quad (1)$$

With

$$\omega_o = \frac{1}{\sqrt{L_p \cdot C_M}} \quad (2)$$

It can be seen that, with a value of $L_p = 560uH$ and $C_M = 1nF$, the previous equation is dominated by the sine term. The output capacitance C_M is not a fixed value or even a linear capacitance, but the error produced by assuming a fixed value capacitance is negligible and only noticeable at the beginning of the "off" time, when the drain voltage is low and therefore C_M peaks in capacitance. Fig. 2 shows the *Spice* simulation of the quasi-resonant waveform. In this figure it can be seen that the drain voltage when M_{SW} turns on has drop to less than 30V. Fig. 3 shows the case where the magnetising inductance L_p has not been tuned to resonate with C_M at the switching frequency ($L_p = 2mH$) and therefore the drain voltage at turn-on is around 150V, producing a very high *dv(t)/dt* and therefore high radiated noise.

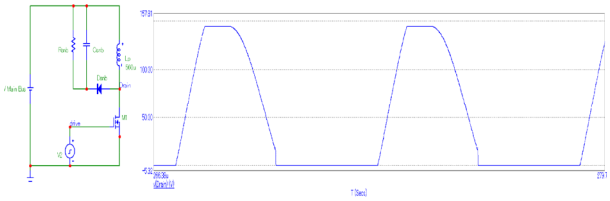

Figure 2. Quasi-Resonant waveform at the drain of the switching MOSFET

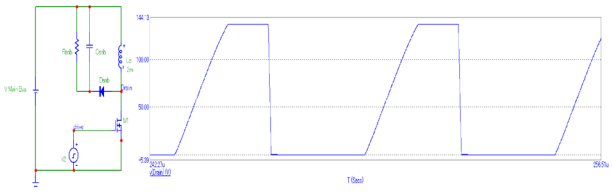

Figure 3. Hard-Switched waveform at the drain of the switching MOSFET (without quasi-resonance)

The main drawback of this topology is the high voltage reached at the drain of the switching MOSFET during the "off" time. This voltage occurs due to the volt/second reset of the magnetising inductance L_p when M_{SW} turns off. Ideally, and for a 50% duty-cycle clock signal, this voltage becomes twice the input voltage. In reality, due to switching delays of M_{SW}, the voltage reached at its drain is higher than twice the input voltage reaching values as high as three times the input voltage. This effect is further exacerbated due to the slow transitions introduced by the quasi-resonant switching. Because of this, an R-C-D snubber has been introduced to keep the drain voltage below its de-rated maximum value. This snubber circuit can be seen in Fig. 2 and Fig. 3.

2.3 Output Series Regulators

As with most multi output converters the outputs are series regulated as follows:

- The +5V, -5V and 3.3V outputs are regulated using an RHFL4913 integrated circuit from STMicroelectronics. It is a Rad-Hard linear regulator IC.
- The 40V series regulator was designed using very basic discrete components.
- For the 1.8V regulator a novel regulation technique was used to achieve very fast feedback current control to limit the over-voltage spike when an SET (Single Event Transient) occurs.

2.4 The 1.8V Output Linear Regulator

The problem with conventional linear regulators, like the RHFL4913, is that if a SET occurs that switches on the main power transistor, even for a short period of time of 1µsec, then the result is a voltage spike that can destroy a sensitive load. One such load is the FPGA being supplied by the 1.8V regulator. A SET may have a duration of 1µsec but can have this period expanded due to capacitive storage or saturation. Since the linear regulator is an analogue device this expansion is most significant when the SET occurs in the voltage feedback loop. We have therefore performed a *Spice* simulation on the discrete 1.8V linear regulation to indicate what improvement can be made for a SET. The SET has been simulated by two pulse generators, one of 1µsec period and another one of 10µsec period. The 1µsec pulse is injected directly on the gate-source of the power MOSFET. The period of 1µsec is used because there is virtually no possibility of pulse expansion at this point. The 10µsec pulse is injected at the output of the operational amplifier that controls the voltage loop.
Fig.4 shows the resulting waveforms for both the above cases and, for comparison, with and without the added second current loop. It is clear that the new design has a major impact on the ability to withstand SET's. SET tests were performed on the breadboard of the converter to confirm the results of the *Spice* simulation. These results are shown in Section 3.

2.4.1 Noise Attenuation

Fig. 5 shows the simulated attenuation achieved. This is around 55dB at 168 kHz which is the frequency of interest because of the ripple voltage coming from the

converter supply. In Fig. 6, the input and output waveforms were simulated with a 200mV peak-peak ripple at the input. The result shows that the resulting ripple voltage at the output level is about 325µV. This confirms the 55dB or rejection.

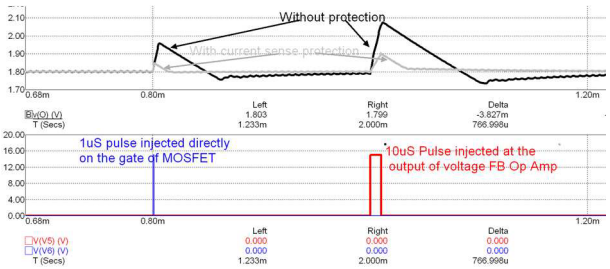

Figure 4. Response of the 1.8V linear regulator to a simulated SET

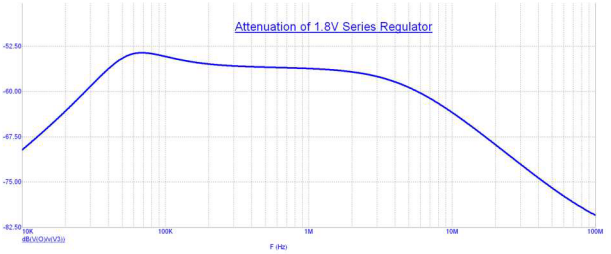

Figure 5. Voltage ripple attenuation of the regulator

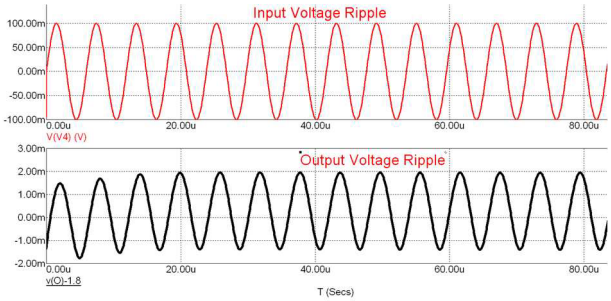

Figure 6. Comparison of the input and output voltages of the 1.8V linear regulator

2.4.2 Headroom

The headroom was tested on the *Spice* circuit by variation of the input supply voltage and monitoring the output voltage. Fig. 7 shows this response, where it can be seen that the headroom required is about 80mV.

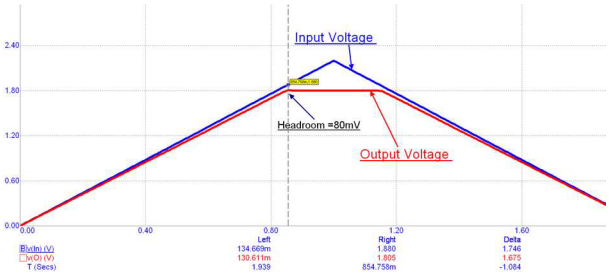

Figure 7. Headroom required for the 1.8V regulator

2.4.3 Load Response

The simulation of load change is shown in Fig. 8. The output voltage response shows a well damped proportional-plus-integral feedback with a voltage overshoot of about 30mV.

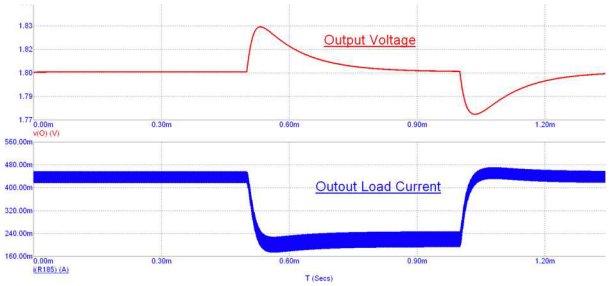

Figure 8. Step load response on the 1.8V output with a 50% load change

2.4.4 Feedback Stability

The voltage feedback open-loop response is shown in Fig. 9. This results in a phase margin of 75° at 119 kHz. Also the transient response with load confirms this stable response.

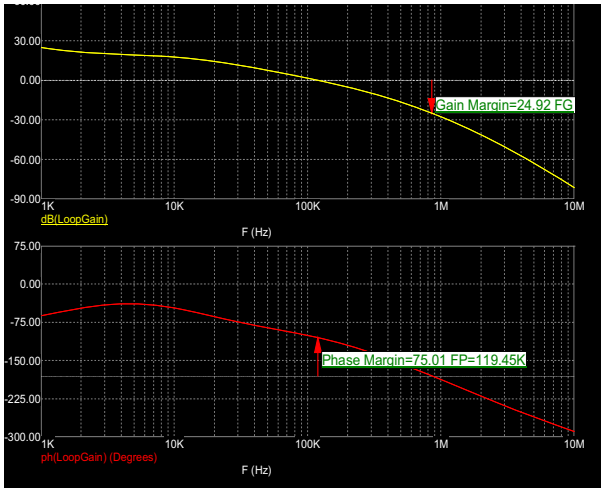

Figure 9. Open-Loop response of the 1.8V regulator

2.5 Input Filter

The input filter was designed to give a 30dB attenuation of conducted ripple current. To satisfy the conducted noise requirements a PI filter was required. This design has been simulated with two values of input harness inductance ($L_{Harness}$), 1µH and 5µH, and is shown in Fig. 10. The resonant peak of the curves is due to the resonance of the harness inductance with the first 500nF input capacitance (C_{PI1}, see Fig. 1) as per Eq. 3.

$$\omega_{peak} = \frac{1}{\sqrt{L_{Harness} \cdot C_{PI1}}} \qquad (3)$$

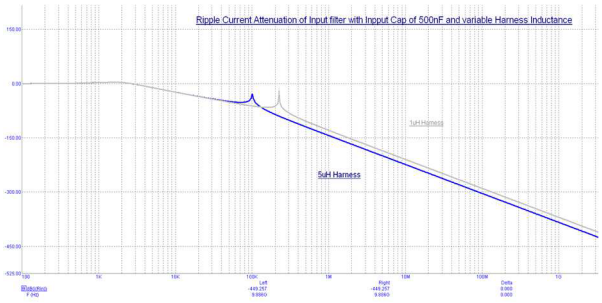

Figure 10. Input filter response

3. RESULTS

The prototype was tested by Clyde Space Ltd. Fig. 11 shows the quasi-resonant waveform on the drain of the main switching MOSFET. In this figure it can be seen the sloping edges of the quasi-resonant waveform and the voltage clamping action provided by the R-C-D snubber shown in Fig. 2 and Fig. 3. It can be appreciated that the drain voltage drops to only 10V before the MOSFET turns-on. The voltage waveform shown in Fig. 11 resembles the waveform produced by the *Spice* simulation shown in Fig. 2. Fig. 2 shows the case where the MOSFET is modelled with a fixed value output capacitance whereas Fig. 11 shows the voltage signature with the actual EM hardware. Any differences are thought to be due to the non-linear capacitance of the switching MOSFET.

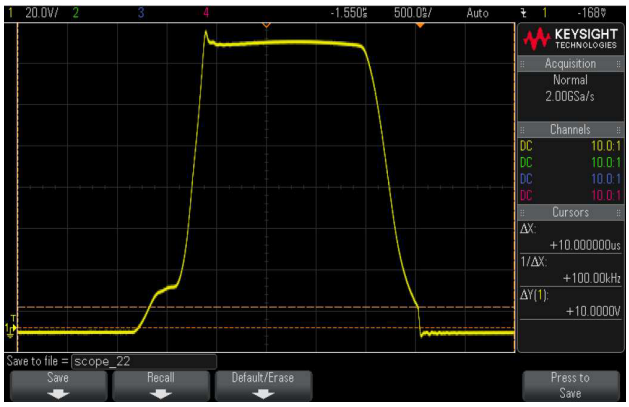

Figure 11. Quasi-Resonant waveform at the drain of the switching MOSFET

The converter passed all the tests for Conducted Emissions and Conducted Susceptibility. These tests were conducted by Selex ES.

The SET test for the OpAmp of the 1.8V regulator was tested injecting two different pulses to the gate of the MOSFET of the linear regulator. The pulses have an amplitude of 10V and a duration of 1µsec and 10µsec, in accordance with the simulations performed and shown in Fig. 4. Fig. 12 and Fig. 13 show the responses of the 1.8V linear regulator to the 1µsec and 10µsec pulses, respectively.

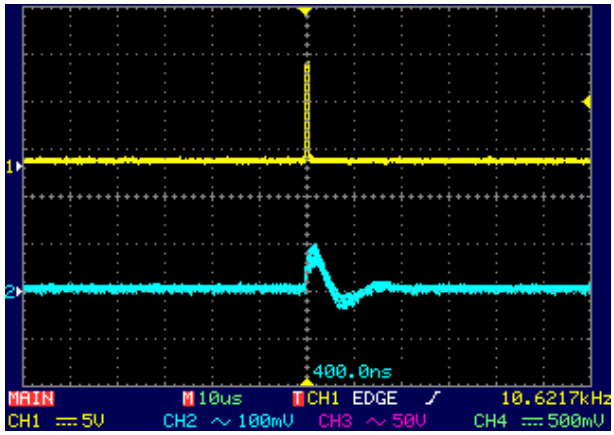

Figure 12. Response of the 1.8V linear regulator to a simulated 1µsec SET

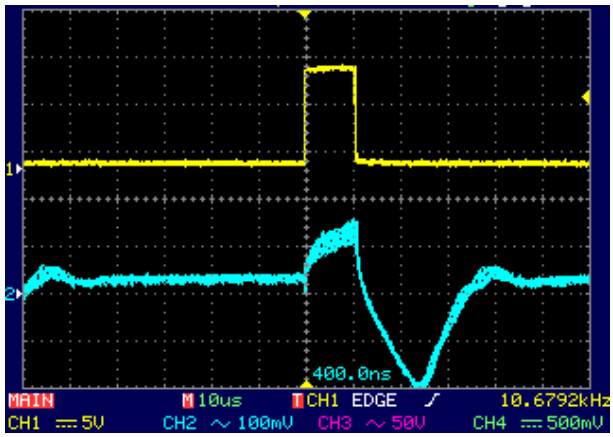

Figure 13. Response of the 1.8V linear regulator to a simulated 10µsec SET

Noise transparency from the input of the PSU to the rectified outputs, at the input of the linear regulators, has been measured in order to check the noise attenuation provided by the converter's input stage. A sinusoidal signal with an amplitude of 1V peak-to-peak and a frequency equal to, approximately, the critical frequency (14.7 kHz) has been injected in series with the converter DC input voltage and the AC coupled noise has been measured at the input of each one of the output linear regulators. Fig. 14 shows the measurements taken at the input of the 1.8V linear regulator, which is the most critical one. It can be observed that the noise transmitted to the input of the linear regulator is 40mV, approximately, for an input AC signal of 1V peak-to-peak.

The load step response test was also performed in all the outputs. The outputs were varied by steps between 100% and 50% of the nominal load currents. Fig. 15 shows the performance of the 1.8V output when the load current changes between 440mA and 220mA. Very small overshoots of less than 50mV have been measured.

The outputs provided by the RHFL4913 linear regulators have step load responses with overshoots of less than

100mV. The 40V output has overshoots of 550mV.

Figure 14. Noise transmitted by the input stage. CH1: Input injected at the input of the converter. CH2: AC signal measured at the input of the 1.8V linear regulator

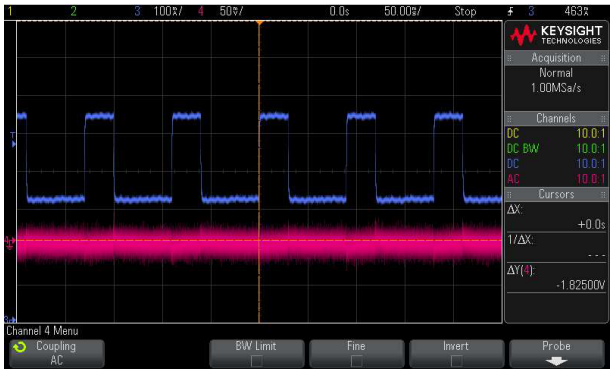

Figure 15. Step load response of the 1.8V output. CH3: Current steps between 100% and 50% nominal output current. CH4: AC coupled voltage at the output of the regulator

Fig. 16 shows the Engineering Model of the PSU assembled inside the SiREUS sensor avionics box. The final solution comprises a mother board and a daughter board with the filter components and the LCL on just one side. The need for a daughter board comes from the small PCB surface area available for the design.

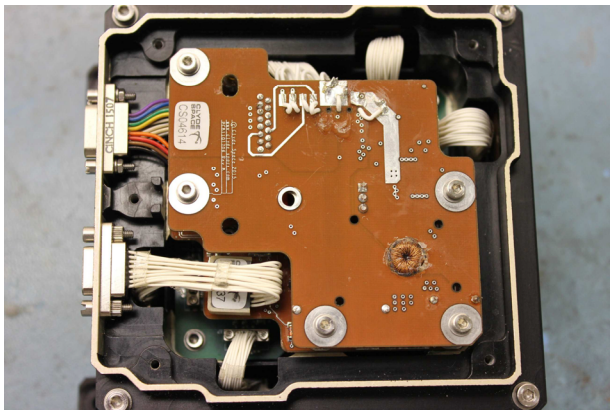

Figure 16. EM of the PSU assembled in the SiREUS CRS avionics box

4. CONCLUSIONS

This paper presents a power converter that has been custom-designed for very stringent low conducted and radiated noise requirements with the restraint of a small PCB volume. The operation from a regulated bus input voltage without PWM control allows a quasi–resonant power stage to be used that has considerably reduced radiated noise. The topology used has proved to be the right choice since the EM, when integrated with its CRS load passed all its noise tests. Also, without PWM control the converter has less failure modes and therefore requires less protection circuits, than a more conventional PWM converter.

The 1.8V supply for the FPGA load has overcome the major disadvantages of the RHFL4913 IC with regard to headroom and SET sensitivity.

The main disadvantage of using an unregulated power stage is low efficiency but, because of the low power required, this is not a concern.

5. REFERENCES

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