WATKINS-JOHNSON TOPOLOGY INTEGRATED IN A FULL-BRIDGE CONVERTER

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ABSTRACT

Electrical thrusters require high power and High Voltage (HV) of 300V to 2000V depending on the thruster technology. A converter suitable for this application should have a high power handling capability (full bridge converter) and a simple output stage (fly-back converter). Other desirable characteristics would be: simplicity, able to supply a wide range of loads, low stress on switches, high stability and galvanic isolation between input and the output power.

The Watkins-Johnson (W-J) topology is used mainly in HV applications due to the fact that its magnetic elements are on the input side. However the power output of this converter is constrained by the "single switch topology". Further downsides of the basic W-J topology are the relatively high voltage stress on the switching elements and the fact that is not galvanically isolated .

This paper will present a new topology of a Full Bridge Isolated Converter which is based on the W-J topology. Steady state behaviour in Continuous Current Mode (CCM) and in Discontinuous Current Mode (DCM) will be investigated. Dynamic performances of the converter will be investigated with the analysis of its transfer function. An equivalent circuit suitable for PSPICE simulations will be presented.

The topology presented potentially offers the following advantages which are suited to providing power conditioning to sub-systems which require high voltage and high power:

- Simple output stage suitable for HV.
- Buck type transfer function, hence simple control scheme.
- Low stress on components.
- Single stage converter
- Suitable for modular high power converter due to the simplicity of the output stage

1. WATKINS-JOHNSON TOPOLOGY

In figures 1 and 2 the W-J topology and a practical realization of it is presented.

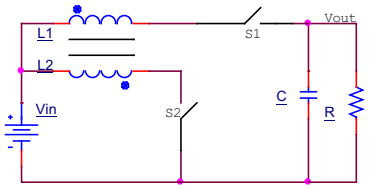

Figure 1. Watkins-Johnson basic topology

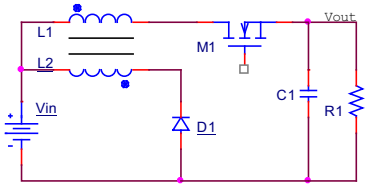

Figure 2. Watkins-Johnson topology practical realization

Its peculiarity is that energy is transferred from input to output during the ON time of M1, while during the OFF time the energy stored in the core of the mutual inductor L1 L2 is given back to the input source.

It can be shown that in CCM the conversion ratio is of the basic topology is (δ refers to duty cycle):

$$\frac{V_{out}}{V_{in}} = \frac{2\delta - 1}{\delta} \qquad (1)$$

Equation (1) is also valid for the practical realization of fig. 2 but only for CCM and δ greater than 0.5.

For the practical realization of fig. 2 the max static voltage stress on the switching elements is 2*Vin. Considering that the input voltage for high power satellites is already 100V and could rise higher in the, this level of voltage stress can seriously limit the choice of power components.

2. ISOLATED VERSION OF THE WATKINS-JOHNSON TOPOLOGY AND ITS INTEGRATION IN A FULL BRIDGE

The isolated version of the topology under study can be implemented as a push pull or full bridge that follows a Watkins-Jonson stage, as depicted in figure 3 and 4.

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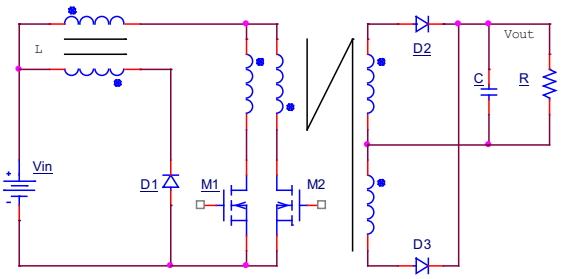

Figure 3. Watkins-Johnson followed by Push-Pull stage

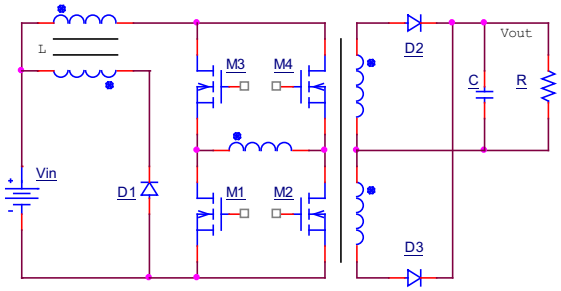

Figure 4. Watkins-Johnson followed by Full-Bridge stage

Despite the introduction of the isolation and the higher power handling capability of the converters in fig. 3 and 4, the conversion ratio is the same as for the basic topology except for a small modification introduced by the transformer ratio $n=N_p/N_s$ where N_p and N_s are respectively the number of the primary and secondary turns of the transformer:

$$\frac{V_{out}}{V_{in}} = \frac{2 \cdot \delta - 1}{n \cdot \delta} \qquad (2)$$

Also the maximum voltage stress on the switching elements is the same as the basic topology, i.e. 2*Vin.

Instead of simply cascading the Watkins-Johnson and a full bridge stage, we can "integrate" the two topologies, as depicted in figure 5. It can be seen that, at the cost of one extra diode on the primary side, the maximum voltage stress on the Mosfets is reduced from 2*Vin to Vin, making the converter suitable for systems based on power busses of 100V or higher.

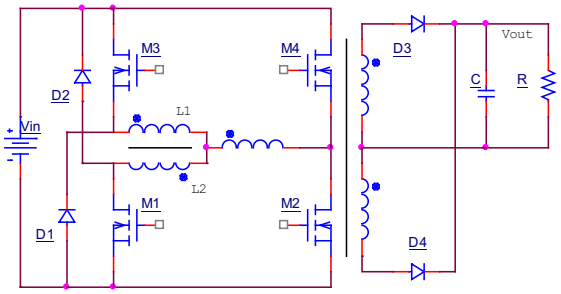

Figure 5. Watkins-Johnson integrated in a Full-Bridge stage

The strong points of this new converter are:

- galvanic isolation
- high power handling capability
- low voltage stress on switches
- simplified output stage

The last point, a simplified output stage, is extremely valuable in case of HV applications and makes this converter a promising candidate for applications like electrical propulsion where high power and high voltage are requested.

It can be also shown that the switches M2 and M4 could operate easily in Zero Voltage Switching (ZVS) mode. The weakest point of this converter is the high input AC current, which will require an adequate filter.

3. CONTINUOUS CURRENT MODE

In continuous current mode, there is always current circulating in the inductor. In this condition the converter operates in 4 phases here described by the names of the switches that are conducting. Referring to fig. 5:

- Phase 1: M3, M2, D3 are ON (and primary current flows in upper inductance branch)
- Phase 2: D1, D2 are ON (and inductor currents recirculates on both inductor branches to the input source)
- Phase 3: M4, M1, D4 are ON (and primary current flows in lower inductance branch)
- Phase 4: D1, D2 are ON (and inductor currents recirculates on both inductor branches to the input source)

Even if the switches are different, phase 1 and 3 are essentially the same, so we can study the CVT considering only phase 1 and 2.

The circuits in phase 1 are depicted in fig. 6 where only the conducting switches have been included. To derive the conversion ratio we will apply the method of the inductor volt seconds balance and the capacitor charge balance under the small ripple approximation [1].

We will use the following convention to distinguish between instantaneous, DC and AC values:
$x = x(t) = X + \underline{x}(t)$
$x = x(t)$: instantaneous value
X : DC value
$\underline{x}(t)$: AC value

In Phase 1 (see fig.6) the governing equations are:

$$v_L = v_{in} - R_L \cdot i_{on} - n \cdot (v_{out} + V_{ds}) \qquad (3)$$

$$i_c = n \cdot i_{on} - \frac{v_{out}}{R} \qquad (4)$$

Where i_{on} is the inductor current, V_{ds} is the voltage drop on the diode on the secondary side, R_L the parasitic resistance of one inductor winding.

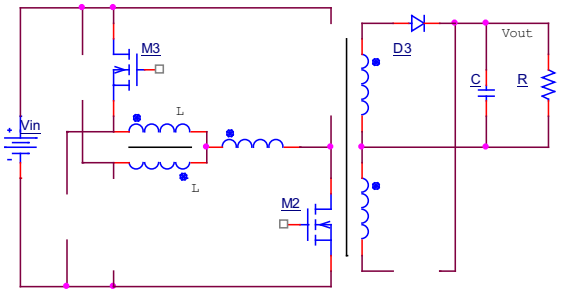

Figure 6. Phase 1 circuit

In Phase 2 (see fig.7) the governing equations are:

$$v_{L_{12}} = -2 \cdot R_L \cdot i_{off} - 2V_{dp} - v_{in} \quad (5)$$

$$i_c = \frac{-v_{out}}{R} \quad (6)$$

Where i_{off} is the inductor current, L_{12} is the inductance of the two windings in series of the mutual inductances, v_{L12} the voltage across L_{12},V_{dp} is the voltage drop on the diode on the primary side.

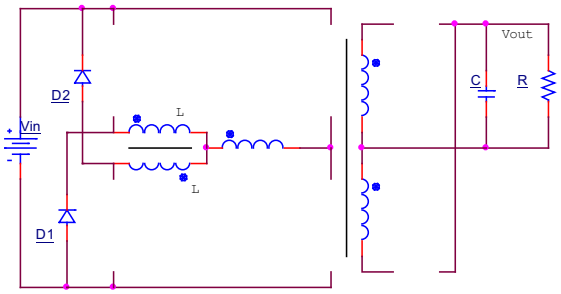

Figure 7. Phase 2 circuit

We now enter in the tricky part of the analysis. In fact the value of the inductance changes between Phase 1 and 2 and in order to apply the principle of VoltSecond balance we have to express V_{L12} in terms of V_L. Considering that:

$$L_{12} = 4 \cdot L \quad (7)$$

(because doubling the number of turn on a core will increase the inductance by a factor of 2^2), and that at the transition times between Phase 1 and 2:

$$i_{off} = \frac{i_{on}}{2} \quad (8)$$

(because the energy in the inductance can't change instantaneously), we can write:

$$v_{L_{12}} = 2 \cdot v_L \quad (9)$$

Substituting (8) and (9) into (5) we have the following governing equations for phase 2:

$$v_L = -R_L \cdot \frac{i_{on}}{2} - V_{dp} - \frac{v_{in}}{2} \quad (10)$$

$$i_c = \frac{-v_{out}}{R} \quad (6)$$

We can now proceed with the Volt Second balance using (3) and (10) and charge balance using (4) and (6) only for the DC values of the concerned variables:

$$0 = \delta \cdot \left[V_{in} - R_L \cdot I_{on} - n \cdot \left(V_{out} + V_{ds}\right)\right] + (1-\delta) \cdot \left(-R_L \cdot \frac{I_{on}}{2} - V_{dp} - \frac{V_{in}}{2}\right) \quad (11)$$

$$0 = \delta \cdot \left(n \cdot I_{on} - \frac{V_{out}}{R}\right) + (1-\delta) \cdot \frac{-V_{out}}{R} \quad (12)$$

From (11) and (12) we can obtain the conversion ratio of the full bridge with the Watkins-Johnson topology, that, in the case the parasitic values R_L, V_{dp} and V_{ds} are zero is:

$$\frac{V_{out}}{V_{in}} = \frac{3 \cdot \delta - 1}{n \cdot 2 \cdot \delta} \quad (13)$$

The conversion ratio modelled by (13) has been plotted in fig.8

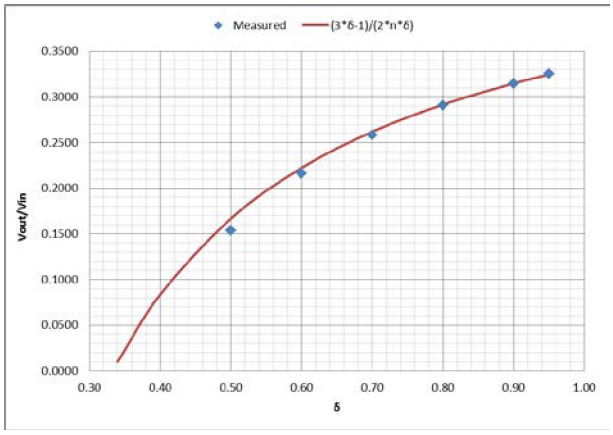

Figure 8. Conversion ratio Vout/Vin(δ) for n=3

4. CONVERTER MAIN WAVEFORMS AND CHARACTERISTICS IN CONTINUOUS MODE

In fig. 9 the major waveforms of the converter in CCM are depicted with reference to the electrical scheme in figure 5.

The major characteristics of the converter in CCM are reported here after.

Input output relationship:
- Vout/Vin=(1/n)*(3*δ-1)/(2*δ)

Switch ratings:
- Drain voltage: Vin
- Peak current: I_Lpk

Primary diodes ratings:
- Voltage: Vin
- Peak current: I_Lpk/2

Secondary diodes:
- Voltage: 2*Vout
- Peak current: (n)*I_Lpk

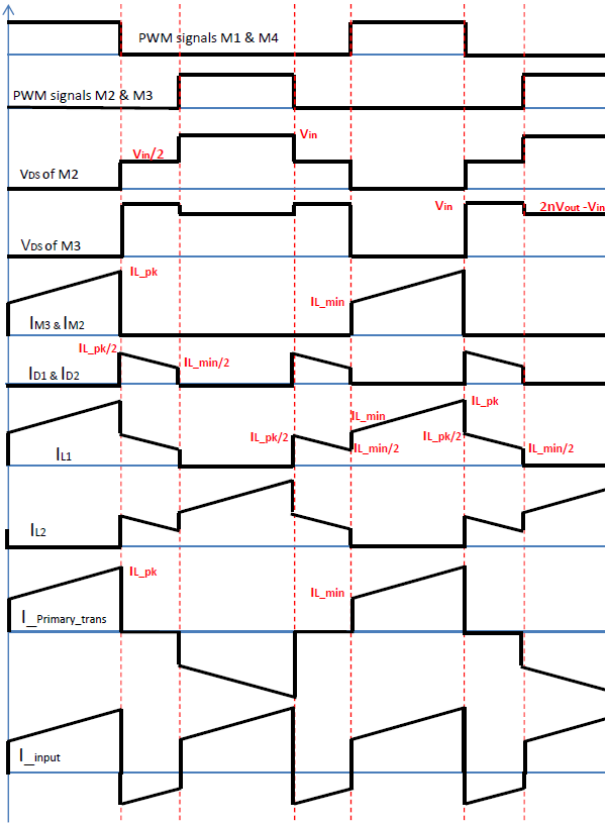

Figure 9. Major waveforms of the converter in the switching period (ideal case)

5. CONTINUOUS AND DISCONTINUOUS MODE BOUNDARY AND K_{crt} and R_{crt}

We know that this converter transfer the current in the inductor to the output only during phase 1, in phase 2 the inductor current goes back to the input source. Hence the average current of the inductor during phase 1 must be the same as the average output current corrected by the transformer ratio. We can then write:

$$I_{L\_avg\_on} = \frac{1}{n} \cdot \frac{V_{out}}{R} \tag{14}$$

Using (13) in (14) and rearranging we have:

$$I_{L\_avg\_on} = \frac{1}{n^2} \cdot \frac{3 \cdot \delta - 1}{2 \cdot \delta} \cdot \frac{V_{in}}{R} \tag{15}$$

On the other hand we know that at the boundary condition between CCM and DCM must be:

$$I_{L\_avg\_on} = \frac{\Delta I_{on}}{2} \cdot \delta \tag{16}$$

From the fig. 6 we can state that

$$\Delta I_{on} = \frac{V_{in} - n \cdot V_{out}}{L} \cdot \delta \cdot T \tag{17}$$

Where ΔI_{on} is the rise of current in the inductor during phase 1 (t on). Using (13) in (17) and rearranging we have:

$$\Delta I_{on} = \frac{1 - \delta}{2 \cdot L} \cdot V_{in} \cdot T \tag{18}$$

Equation (16) also allow us to set the boundary condition between the two modes, for CCM must be:

$$I_{L\_avg\_on} > \frac{\Delta I_{on}}{2} \cdot \delta \tag{19}$$

For DCM must be:

$$I_{L\_avg\_on} < \frac{\Delta I_{on}}{2} \cdot \delta \tag{20}$$

Substituting in equation (19) equation (15) on the left side and (18) on the right side, we get:

$$\frac{1}{n^2} \cdot \frac{3 \cdot \delta - 1}{2 \cdot \delta} \cdot \frac{V_{in}}{R} > \frac{1}{2} \cdot \frac{1 - \delta}{2 \cdot L} \cdot V_{in} \cdot T \cdot \delta \tag{21}$$

Rearranging (21):

$$\frac{2 \cdot L}{n^2 \cdot R \cdot T} > \frac{(1 - \delta) \cdot \delta^2}{3 \cdot \delta - 1} \tag{22}$$

Defining:

$$K = \frac{2 \cdot L}{n^2 \cdot R \cdot T} \tag{23}$$

$$K_{crt}(\delta) = \frac{(1 - \delta) \cdot \delta^2}{3 \cdot \delta - 1} \tag{24}$$

We have that we are in CCM if:

$$K > K_{crt}(\delta) \qquad (25)$$

Equation (24) predicts that for δ=1/3 K_{crt} will be infinite so the converter will be always in DCM, which is correct because from (13) Vout is zero for δ=1/3 so no current in the inductor at all since the load is zero Watts.

For δ<1/3 K_{crt} equation (25) loses its meaning and the converter will be always in DCM. Rearranging (22) we can define $R_{crt}=R_{crt}(\delta)$.

$$R < \frac{2 \cdot L}{n^2 \cdot T} \cdot \frac{3 \cdot \delta - 1}{(1-\delta) \cdot \delta^2} \qquad (26)$$

$$R_{crt}(\delta) = \frac{2 \cdot L}{n^2 \cdot T} \cdot \frac{3 \cdot \delta - 1}{(1-\delta) \cdot \delta^2} \qquad (27)$$

Equation (27) has been plotted in fig. 10, under the assumption of L=70uH, T=5us and n=3. The Y axis is R_{crt}. In order to be in CCM, R of the load must be lower than R_{crt} plotted.

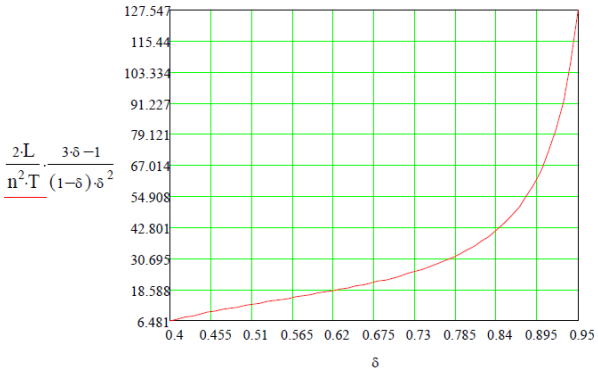

Figure 10. Plot of $R_{crt}(\delta)$for L=70uH, T=5us and n=3

6. CONVERTER MAIN WAVEFORMS AND CHARACTERISTICS IN DISCONTINUOUS CURRENT MODE

In the following figure the main waveforms of the converter in DCM are reported with reference to the electrical scheme in figure 5.

The major characteristics of the converter (Voltage and Current stress levels) in DCM are essentially the same as in CCM, as can be seen in figure 11.

The converter gain in DCM is given by the following formula in the ideal case:

$$\frac{V_{out}}{V_{in}} = \frac{\delta^2}{n \cdot (K + \delta^2)} \qquad (28)$$

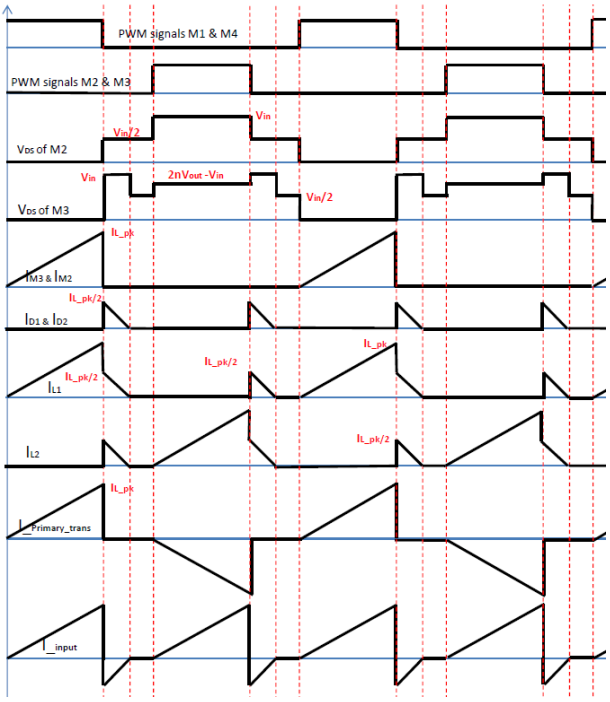

Figure 11. Major waveforms of the converter in the switching period when in CCM (ideal case).

7. MEASUREMENTS

Figure 8 shows measurements of Vout/Vin compared to duty cycle, measured at Vin = 100V, n=3, Pout=50W. It is observed that the measured results follow the derived formula, allowing for a slight error due to voltage drop in the output diodes.

A breadboard of the converter in fig. 5 was configured in closed loop using a UC1825 PWM controller which utilises peak current control. The breadboard was designed for Vin=100V, Vout=30V, fsw=100kHz and max Pout=500W.

Although this topology has been identified as suitable for HV, for the first iteration a low 30V output voltage was selected in order to simplify the testing and debugging.

Figure 12 shows some waveforms measured on the converter working at 113W. It is observed that the general shape of the measured waveforms corresponds to those found in Figure 9. The discrepancies are due to parasitic effects, in particular, the ~1.8MHz damped oscillations (seen on the inductor current and $V_{DS(M3)}$) are due resonance of the transformer leakage inductance with the parasitic capacitance of the Mosfets. These oscillations can be reduced or removed using an RC snubber across each Mosfet.

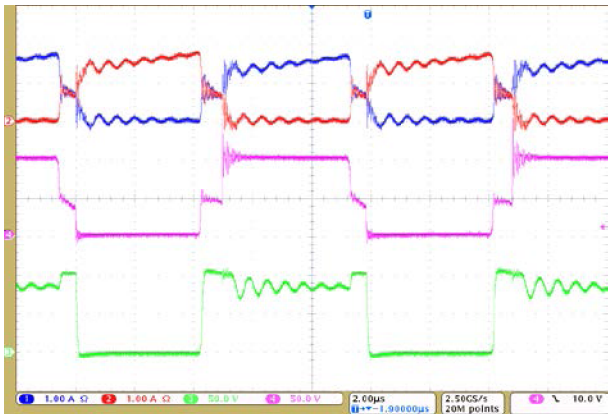

Figure 12. Measured waveforms in CCM: I_{L1}(red), I_{L2}(blue), $V_{D(M2)}$ (pink), $V_{DS(M3)}$ (green) @ Vin=100V, Vout=30V, Pout=113W, fsw=100kHz,

Figure 13 shows the efficiency curve of the breadboard, plotted from a selection of measurements from 15-500W. Above 50W the efficiency is higher than 91% and from 110W-190W it is >94.5%. Above about 380W the converter was operating at maximum duty cycle (96.5%), so without regulation and the output voltage gradually drops with increasing power demand. Note that the breadboard has not been optimised for its highest efficiency, improvements could be made by reducing leakage inductance and resistance in the magnetic components and by selection of different switching components.

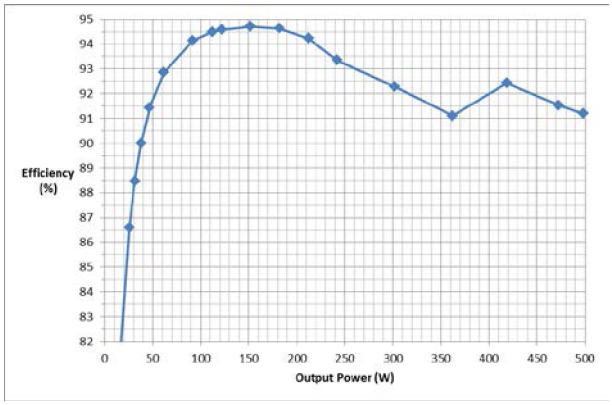

Figure 13. Efficiency curve of the converter @ Vin=100V, Vout=30V, fsw=100kHz

The stability of the converter topology is demonstrated using spectrum analysis which measured phase margin above 60deg and gain margin above 10dB throughout the output power range, including at low power (10W) in DCM. Two bode plots are given to show stability performance at 10W (fig.14) and 200W (fig.15).

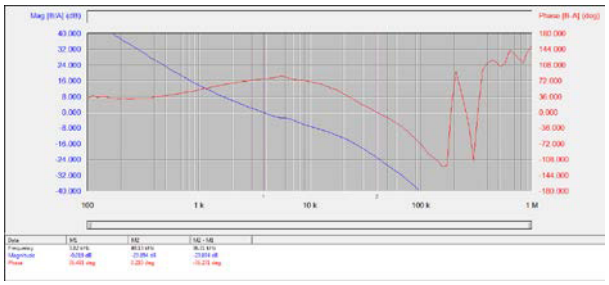

Figure 14. Bode plot at 10W (DCM)

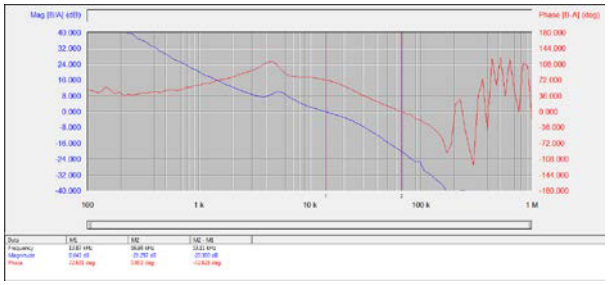

Figure 15. Bode plot at 200W (CCM)

8. CIRCUIT EQUIVALENT MODELLING

We will discuss now a practical and valuable way to model our converter for closed loop simulations without passing through space state averaging and linearization.

Equation (3), (4) for the ON time and (10), (6) for the OFF time, allow us to define an "averaged" equivalent circuit suitable to be simulated in PSPICE.

Averaging equations (3), (4), and (10), (6) and the expressions of the input voltage get:

$$L \cdot \left(\frac{d}{dt} i_{on}\right) = \left(\frac{3 \cdot \delta}{2} - \frac{1}{2}\right) \cdot v_{in} - \frac{(\delta + 1) \cdot R_L}{2} \cdot i_{on} - (1 - \delta) \cdot V_{dp} - \delta \cdot n \cdot V_{ds} - \delta \cdot n \cdot v_{out}$$

(28)

$$C \cdot \frac{d}{dt} v_{out} = \delta \cdot \left(n \cdot i_{on} - \frac{V_{out}}{R}\right) + (1 - \delta) \cdot \frac{-V_{out}}{R} \qquad (29)$$

$$i_{in} = \delta \cdot i_{on} + (1 - \delta) \cdot -\frac{i_{on}}{2} \qquad (30)$$

Rearranged and simplified they become

$$L \cdot \left(\frac{d}{dt} i_{on}\right) = \left(\frac{3 \cdot \delta}{2} - \frac{1}{2}\right) \cdot v_{in} - \frac{(\delta + 1) \cdot R_L}{2} \cdot i_{on} - (1 - \delta) \cdot V_{dp} - \delta \cdot n \cdot V_{ds} - \delta \cdot n \cdot v_{out}$$

(31)

$$C \cdot \left(\frac{d}{dt} v_{out}\right) = \delta \cdot n \cdot i_{on} - \frac{V_{out}}{R} \qquad (32)$$

$$i_{in} = \left(\frac{3 \cdot \delta}{2} - \frac{1}{2}\right) \cdot i_{on} \qquad (33)$$

The equivalent circuit described by (31), (32) and (33) is depicted in fig. 16.

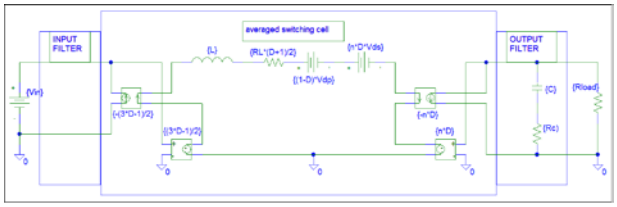

Figure 16. equivalent averaged circuit of the Full Bridge Watkin-Johnson converter.

In the PSPICE model we see three areas: “input filter”, “averaged switching cell” and “output filter”. In the first and latter areas components can be added as wished without considering “averaging” their value.

When adding extra components in the averaged switching cell, we have to “average” them. For example if we want to add the parasitic capacitance of the output diodes, then the actual value to be used in the circuit will be n*D*Cds, where Cds is the capacitance of the secondary diodes.

Using the circuit of figure 16 it is easy simulate a closed loop converter and plot the transfer functions, enabling the study the transient response while modelling the input and output filters. It is worth noting that the circuit in fig. 16 is a non-linear circuit, and it describes both DC and AC behaviour.

9. CONCLUSIONS

- A Full Bridge DC/DC converter based on the Watkins-Johnson topology has been presented and its static characteristics and waveforms in CCM and DCM have been analytically derived.
- A breadboard have been built to verify the analytical work, to study its limitations and to verify the stability of the converter in voltage closed loop.
- An average PSPICE model of the converter in CCM has been also presented.
- The authors believe that this work has confirmed that the Full Bridge W-J converter is a strong candidate for converters for Electrical Propulsion units.

10. SUGGESTIONS FOR FUTURE WORK

Further work should be in the area of:

- loop stability (with current loop)
- study the effect of the “parasitics”
- efficiency optimization (conditions for partial ZVS operations)
- HV output stage
- develop a modular approach to increase output power

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