TWO-DOMAINS CONTROL OF A BUCK CONVERTER

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ABSTRACT

In the design of a power converter, the maximum output voltage transient under load change is one of the main drivers. The ECSS-E-ST-20C imposes specific requirements on the power quality of a regulated bus, which result most of the time in the use of a large capacitor bank to cope with the linear loop dynamics. Moreover, this sometimes results in slow dynamic response.

In this paper a combined linear and non-linear control applied to a buck converter is proposed. This control technique enhances the transient performance with a faster recovery time and allows smaller output filter capacitors to be used. The proposed control is a combination of a linear control based on a conductance control principle, and a non-linear control, which intervenes only during transients. The latter is based on the detection of the output voltage variation and on the immediate application of maximum or minimum inductor current, as consequence of voltage undershoot or overshoot. Once the controlled output voltage is within the allowed range, the linear control takes back the voltage regulation control.

The buck converter is chosen as a reference topology since most of the current solar array regulators (SARs) use a buck or super buck topology. Most Battery Discharge Regulators (BDRs) are also based on buck-derived topologies.

This concept can find application in the three-domain regulated bus control.

1. INTRODUCTION

The proposed control technique is called “two-domains” because it is given by the combination of a linear control, called conductance control, well described in [5] and widely used in space, and a non linear part (called NL-control in the present paper), which is based on the detection of the output voltage variation and comparison of this variation with a pre-determined threshold. During a load transient, in case the output voltage crosses a threshold, the NL-control is activated and forces maximum or minimum inductor current. As soon as the linear control recovers its dynamic, the linear part of the modulating signal takes back control of the converter. In this way the converter works with fixed frequency in steady-state operation and for small signal variation the behaviour is linear.

In case of large load-steps, the operation of the converter is similar to a hysteresis control around a well-defined reference.

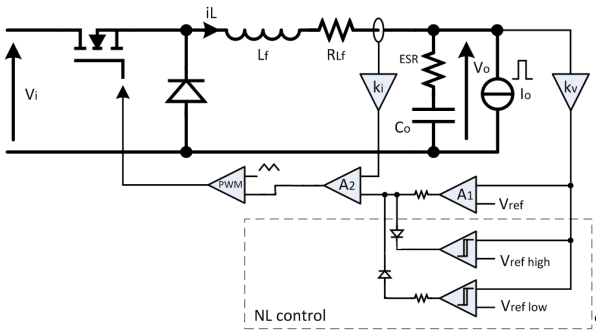


Figure 1: Generic block diagram for the two domain control scheme.

The objective of the proposed work is to design a system satisfying the following criteria:

- Enhanced step load response
- Lower output capacitance when compared to converters with conventional control
- Power quality, transient, ripple and stability requirements as per ECSS-E-ST-20C

1.1 Example of application

We can take as reference a 300 W buck converter providing a regulated 28 V output from an input voltage of 36 to 50 V. For such a system , ECSS-E-ST-20C imposes 1 % bus voltage variation for 50 % load change and 5 % variation under any other load change and inter-domain application. The maximum impedance that the converter can have is given by:

$$Z_0 = \frac{0.02V_0^2}{P_0} \quad (1)$$

For our example application the result is 52 mΩ. For a well-designed conductance control, the maximum output impedance is given by:

$$Z_0 = \frac{1}{k_v A_1 G} \tag{2}$$

Where k_v is the output voltage sensing gain and A_1 is the voltage loop controller proportional gain, as shown in *Figure 1*. G is the conductance of the power stage under closed loop conductance control. Assuming a high-bandwidth current loop, it can be approximated with the following equation:

$$G = \frac{1}{k_i} \tag{3}$$

Where k_i is the gain of the current sensor. The same well-known design criteria for a conductance control also implies the following:

$$C_0 = \frac{k_v A_1 G}{2\pi f_{BW}} \tag{4}$$

where f_{BW} is the desired bandwidth of the converter, which might be initially set to about 1/10 of the switching frequency. For a 300 W converter, we can suppose that a switching frequency of around 100 to 150 kHz is adopted in order to keep the losses low. This results in a bandwidth in the order of 10 to 15 kHz.

$$C_0 = \frac{1}{Z_0 2\pi f_{BW}} \tag{5}$$

which implies a capacitance of more than 300 µF. In a control system that features a non-linear part, which acts during transients and ideally has an infinite gain, such as the one of a comparator used in a hysteresis control, the output impedance is in theory close to zero, if Eq. (2) is taken as reference.

The transient performance is therefore mainly dominated by the output filter dynamics, i.e. the voltage variation across the capacitor due to the current ripple.

It is worth noticing that the NL-control can be designed to act on the set point of the current loop and not directly on the duty cycle. It is also possible to inject the NL signal at several places in the loop, as shown in *Figure 1*. In this case it is combined with the voltage loop, to change the reference of the current loop as fast as possible. This approach also allows to limit the current in case of overload.

In the following paragraph the design criteria for the combined conductance and NL-control are presented.

2. DESIGN CRITERIA

The converter topology that is considered is a buck converter. The design criteria of a buck converter are well-known. In particular, the design of the output capacitor, based on the maximum ripple requirement in steady state and on the maximum voltage variation during step load. The driving requirement is generally the maximum variation under step-load.

The proposed NL-control part, shown in Figure 1, can be explained looking at *Figure 2*. It consists of two comparators with hysteresis that detect if the output voltage is higher (or lower) than a pre-determined threshold V_{tr_high} (or V_{tr_low}). When this happens, a command called V_{cmd_high} (or V_{cmd_low}) is sent and combined with the voltage control loop signal. This command will therefore impose full (or minimum) current.

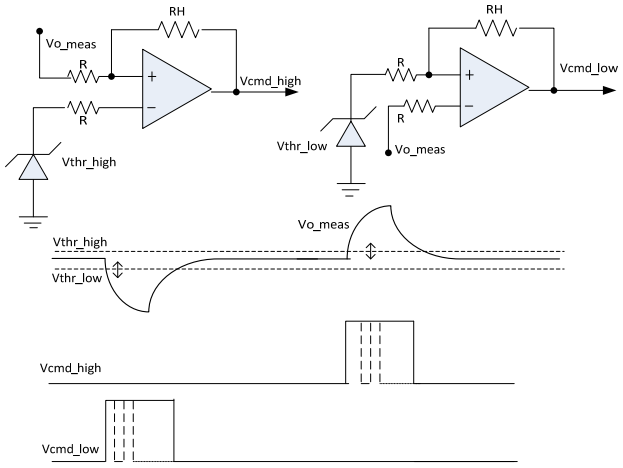


Figure 2: NL-control comparators

This results in a form of hysteresis control applied on the output voltage for a certain period of time, until the linear control dynamic takes back control of the voltage regulation.

2.1 Output capacitor design criteria

The main requirement that is considered for the design of the buck output capacitor is the allowed transient during 50 % step load, which is 1 %. During this operation mode, the NL-control part takes the lead and imposes a sudden change in the current reference, i.e. maximum (or minimum) current. This will result in full (or eventually the one limited by the control circuitry) (or zero) duty cycle. The inductor current will ramp up (or down) imposing the same AC current variation in the output filter capacitor.

As described in [2], the minimum achievable output voltage transient appearing at the onset of an overload is:

$$\Delta V_o = \frac{\Delta I_o^2 L_f}{2(V_{in} - V_o) \cdot C_o} \quad (6)$$

for undershoot and:

$$\Delta V_o = \frac{\Delta I_o^2 L_f}{2 V_o C_o} \quad (7)$$

for overshoot, with ΔI_o being the load (=inductor current) step and L_f the buck inductor value.
In a buck converter, the worst-case transient is the undershoot case. The minimum value of output capacitance necessary for achieving a given ΔV_o is therefore calculated considering the Eq. (6).
Targeting ΔV_o to be less than 0.01xV_o:

$$C_0 \geq \frac{\Delta I_o^2 L_f}{0.02 V_o (V_{in} - V_o)}, \quad (8)$$

which becomes:

$$C_0 \geq \frac{\Delta I_o^2 L_f}{0.02 V_o (V_{in,\min} - V_o)}, \quad (9)$$

The actual ΔI_o varies with the exact moment the transient occurs. The worst case occurs when the inductor current is at the end of the switching period and the MOSFET is OFF. For example, if the load changes form 50% to 100% load and the MOSFET is OFF, without taking into account other delays, the overall ΔI_o in the Eq.(7) becomes: $\frac{I_0}{2} + I_{0,ripple,pk-pk}$.
The bigger the ripple, the deeper the transient and a bigger capacitor needs to be used.

Moreover, to get the minimum voltage variation it is desirable to have the minimum hysteresis in the NL-control as well as minimum delays in the feedback path (for example due to the comparators and to the driver). In fact all these factors result in additional contributions to the output voltage variation. For example the hysteresis band contribution ΔV_{hyst} will result in an increase of the voltage variation of $\frac{\Delta V_{hyst}}{k_v}$.
In principle, the faster the voltage detection and the entire chain of commands, the smaller the resulting voltage transient during application of the NL control.

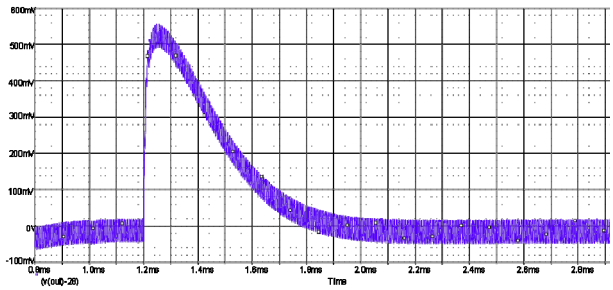
3. SIMULATION RESULTS

Before presenting experimental results, let us show some simulation results. The case study that has been bread-boarded (and simulated) is a converter of 300 W maximum power, 36 - 50 V input voltage range and 28V output voltage. The control system consists of a conventional conductance control, with conductance gain $G = 0.36$, $k_v = 0.118$ and sized in order to have 60° phase margin. The voltage loop control signal is also combined with the output of the two comparators described in paragraph 2.

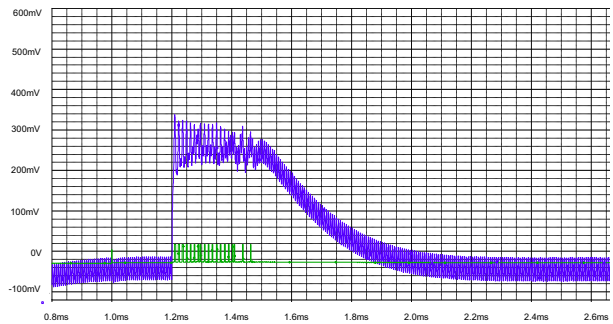
The PWM switching frequency is 300 kHz and the inductor is 13 µH. According to Eq.(8), the output capacitor shall be greater than 80 µF. A capacitor 85 µF has been used in the simulation and in the breadboard.

Figure 3 and *Figure 4* show the transient performance when 50 % load change is applied (100%full load to 50% in *Figure 3* and viceversa in *Figure 4*), without NL-control (figure (a)) and with NL-control (figure (b) and (c)). The blue track is the output error signal V_o-V_{ref} and the green one is the output of the NL-comparators. In Figures (b) and (c) the NL-comparator thresholds V_{tr_high} and V_{tr_low} shown in *Figure 2* have been changed in order to verify the effect.

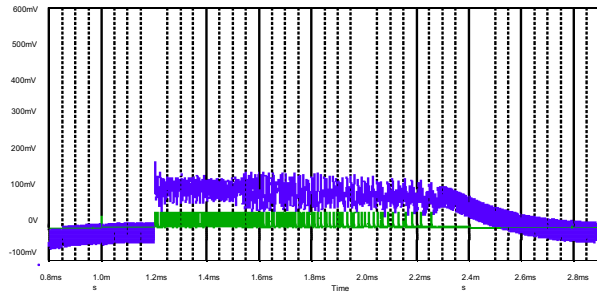
The effect of the NL-control on the overall peak of the voltage variation can clearly be seen.



(a)

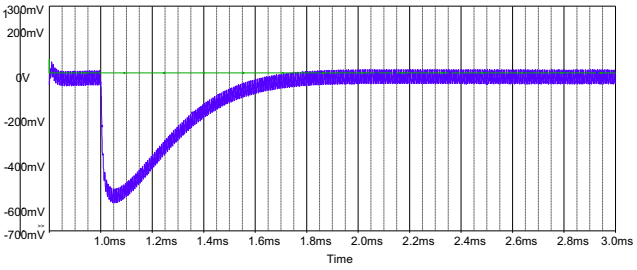


(b)

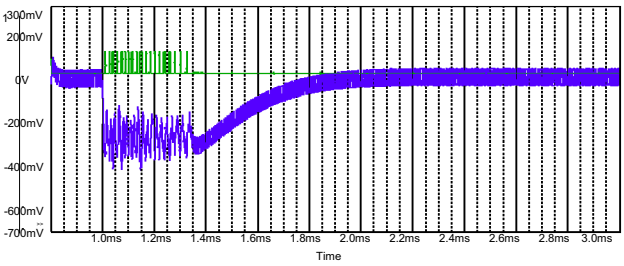


(c)

Figure 3: 100% full load to 50% load transient performances without NL-comparators (figure (a)) and with NL-control at different thresholds ((b) and (c)). Blue: V_o-V_{ref} ; green: NL-comparator output.



(a)



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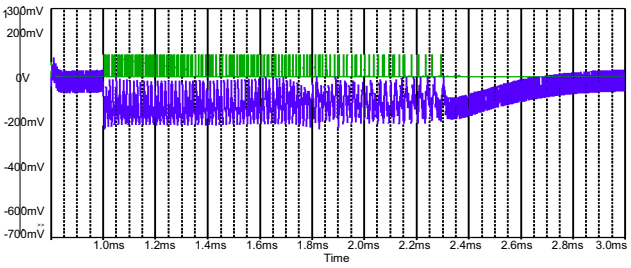

(c)

Figure 4: 50% load to 100% load transient performances without NL-comparators (figure (a)) and with NL-control at different thresholds ((b) and (c)). Blue: V_o-V_{ref} ; green: NL-comparator output.

4. EXPERIMENTAL RESULTS

The converter described in the previous part was built on a PCB in the ESTEC power electronics laboratory. The level of the switching noise needs to be kept very low due to the sensitive nature of the NL control circuits (high speed comparators). This was achieved through the use of ground planes, careful layout of the power cell for low parasitics, controlled switching times for the MFETs and implementation of snubbers. The PWM controller is implemented entirely using discrete components mainly to be able to interface it at several levels with the NL-control circuit part. It is also capable of commanding the power MFETs from 0 % to 100 % duty cycle. The converter also features an output overload protection and a soft start, and reaches an efficiency of 95 % at full load. The prototype is shown in *Figure 5*.

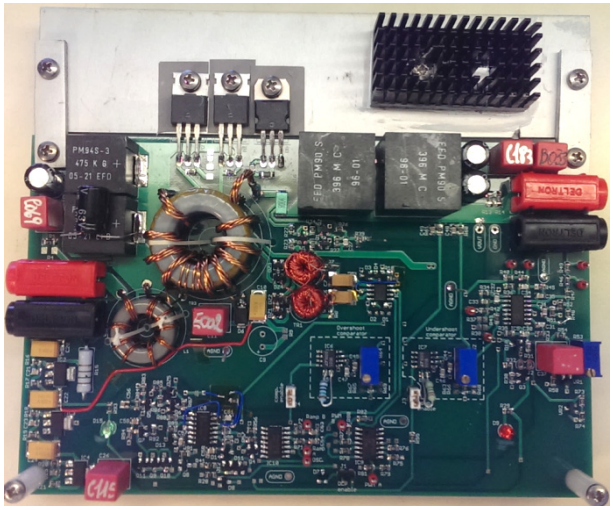

Figure 5: Two-domains buck converter prototype

The voltage loop of the linear control circuit has been designed with a bandwidth of 16kHz and the current loop with a bandwidth of 95kHz. The voltage loop measurements are shown in *Figure 6*.

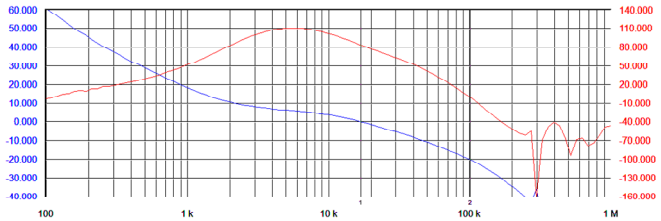

Figure 6: Voltage loop measurements

For the NL-control side, two different methods for detecting the output voltage variation have been used. The first is based on a DC detection, as in a normal conductance control (shown in *Figure 2*), while the other one is based on AC detection, which senses the high-frequency components of the output voltage with a

much higher gain, resulting in better noise immunity (as shown in *Figure 7* with the addition of a capacitor across the high side sensing resistor).

The experimental results of output voltage transient at 50% load change are summarised below for a DC coupled detection and AC coupled one. The magenta trace is the AC output voltage component and the green one is the output of the NL-comparator.

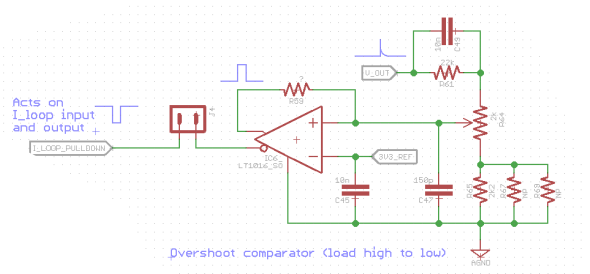

Figure 7: Prototype NL-comparator circuit schematic wired for AC detection.

4.1 DC coupled: Low to High step load tests (50% to 100% load power)

The experimental results show the output voltage transient performance (AC variation) without connecting the NL-comparator (*Figure 8)* and with NL-comparators at three different DC detection thresholds (*Figure 9* to *Figure 11*).

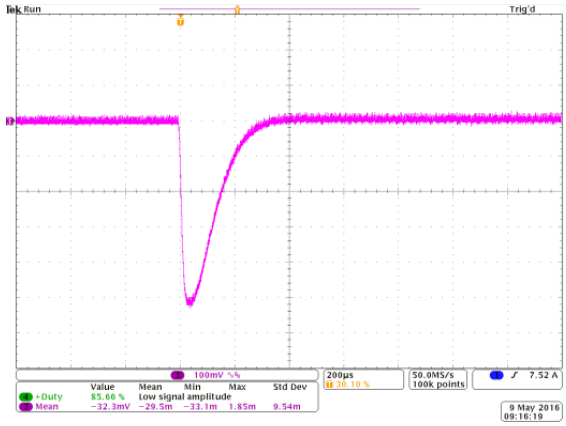

Figure 8: Output voltage transient under 50% to 100% load power change without NL-comparators

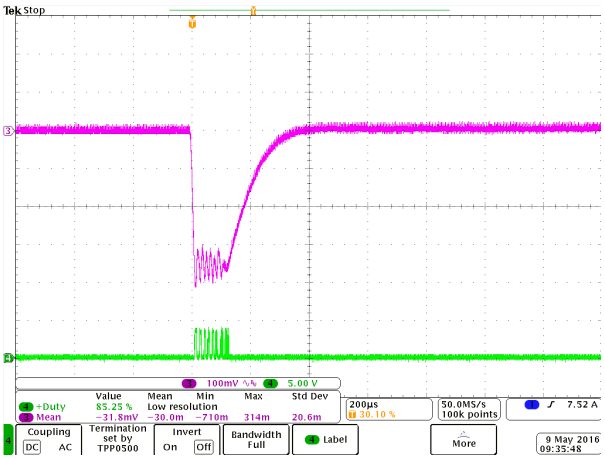

Figure 9: DC coupled output voltage transient under 50% to 100% load power change with NL-comparators

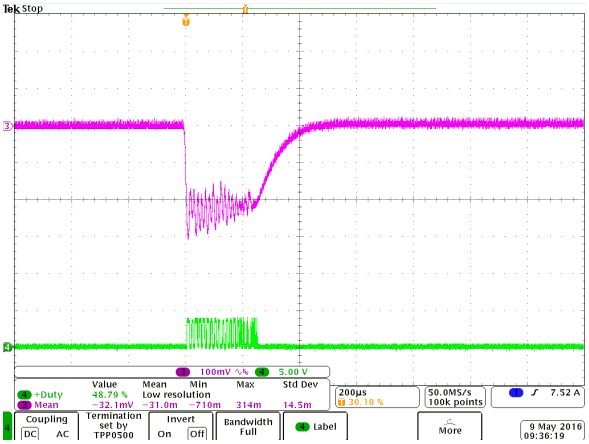

Figure 10: DC coupled output voltage transient under 50% to 100% load power change with NL-comparators

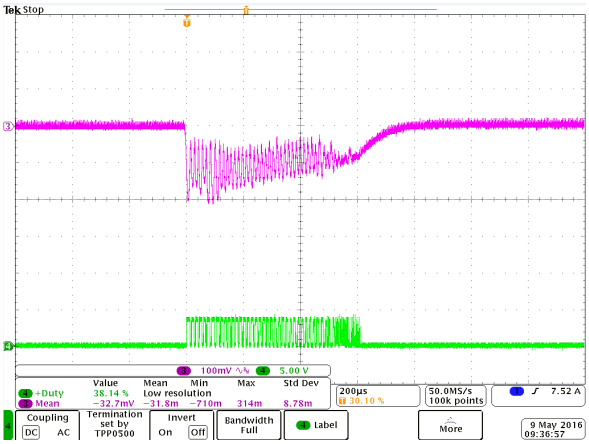

Figure 11: DC coupled output voltage transient under 50% to 100% load power change with NL-comparators

4.2 AC coupled: Low to High step load tests (50% to 100% load power)

The experimental results show the output voltage transient performance (AC variation) with NL-comparators at two different AC variation thresholds (*Figure 12* and *Figure 13*)

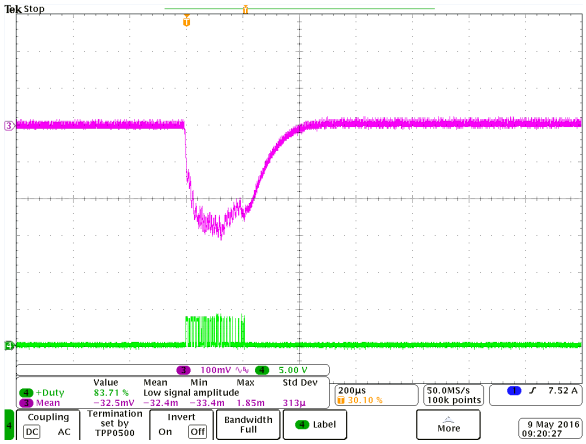

Figure 12: AC coupled output voltage transient under 50% to 100% load power change with NL-comparators

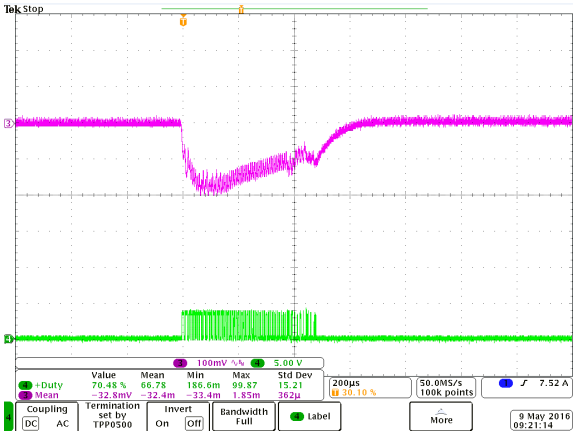

Figure 13: AC coupled output voltage transient under 50% to 100% load power change with NL-comparators

4.3 DC coupled: High to Low step load tests (100% to 50% load power)

The experimental results show the output voltage transient performance (AC variation) without connecting the NL-comparator (*Figure 14*) and with NL-comparators at two different DC variation thresholds (*Figure 15* and *Figure 16*)

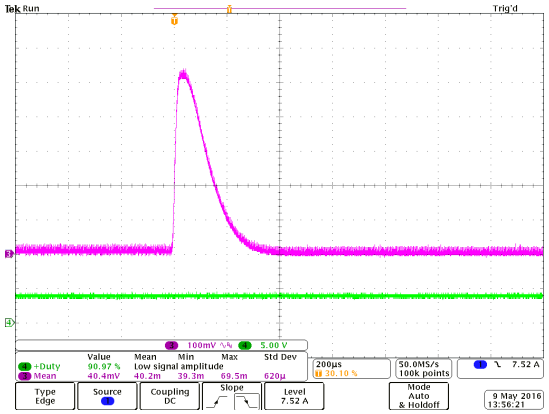

Figure 14: DC coupled output voltage transient under 100% to 50% load power change without NL-comparators

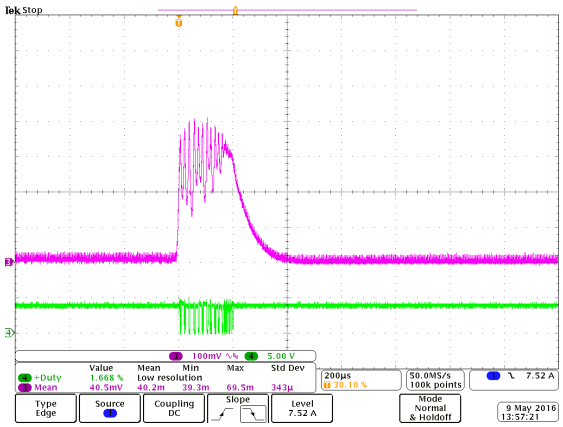

Figure 15: DC coupled output voltage transient under 100% to 50% load power change with NL-comparators

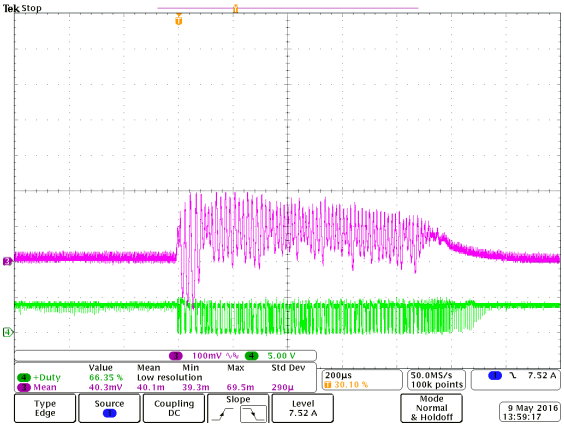

Figure 16: DC coupled output voltage transient under 100% to 50% load power change with NL-comparators

4.4 AC coupled: High to Low step load tests (100% to 50% load power)

The experimental results show the output voltage transient performance (AC variation) with NL-comparator at the smallest reference threshold (*Figure 17*)

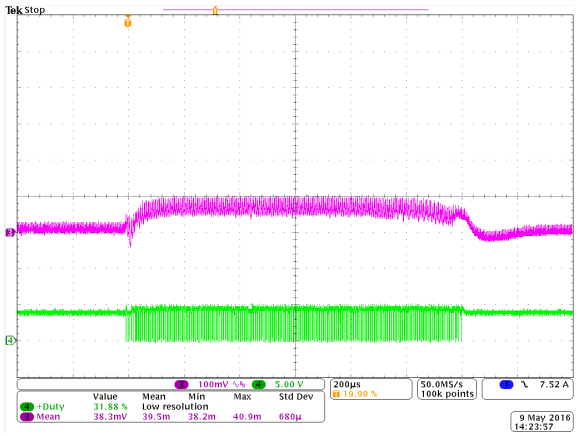

Figure 17: AC coupled output voltage transient under 100% to 50% load power change with NL-comparators

Tests show that the AC coupling gives better results and it will be taken as reference for this type of control.
They also show that this control used 85µF against the min 300µF of a conventional conductance control.

4.5 NL-control ripple characterization

The voltage ripple during the transient NL-control depends on many factors.

In a system where the ESR of the output capacitor is relatively big [3], the ripple reflects the hysteresis of the comparators. Knowing the ESR, the load current and the applied hysteresis window and internal delays it is possible to calculate the frequency.

In our case-study we aim for the best performance in terms of output voltage variation during transition and minimum ripple. This means: the ESR is very small, the hysteresis window is set to be as small as possible and minimum internal delays are aimed. In this case the evaluation of the hysteresis switching frequency becomes very difficult. In a system with zero delays and hysteresis the frequency is in theory infinite. Testing is the best solution for this type of control, where each single delay contribution plays an important role in the performance.

From the testing done on the prototype, it seems that the frequency remains more or less constant with the input voltage, while the ripple of the inductor current slightly changes, as shown in the *Figure 19* and *Figure 18* It can be also seen that the current ripple is given by:

$$\Delta I_{ripple} \approx \frac{\left(V_{in} - V_o\right) V_o T_{hyst}}{L_f V_{in}} \qquad (10)$$

where T_{hyst} is the period of oscillations. The current ripple is indeed around 6.5A in one case and the half of that in the other one.

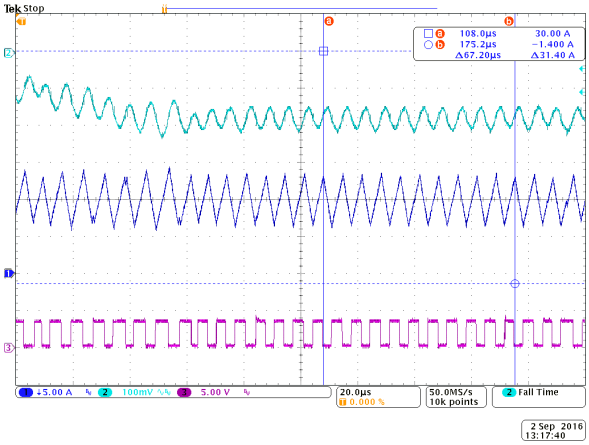

Figure 18: 50% to 100% load transient: output voltage error (light blue), inductor current (blue), NL-comparator signal output (magenta)@50V input

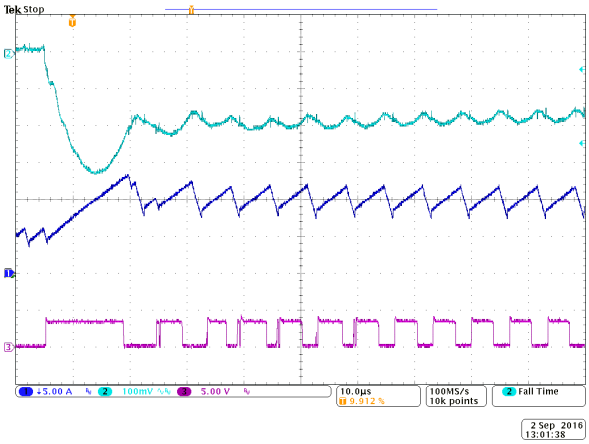

Figure 19: 50% to 100% load transient: output voltage error (light blue), inductor current (blue), NL-comparator signal output (magenta)@36V input

The output capacitor ripple during the NL-control can also be characterized with the following formula:

$$\Delta V_0 = \frac{\Delta I_{ripple}}{8C_0} T_{hyst} \qquad (11)$$

It is in fact linked to the current ripple, as can be seen in *Figure 20*, where the $\Delta I_{ripple,}$ is 6A and T_{hyst} is 6.8µs. The ΔV_0 is indeed 57mV.

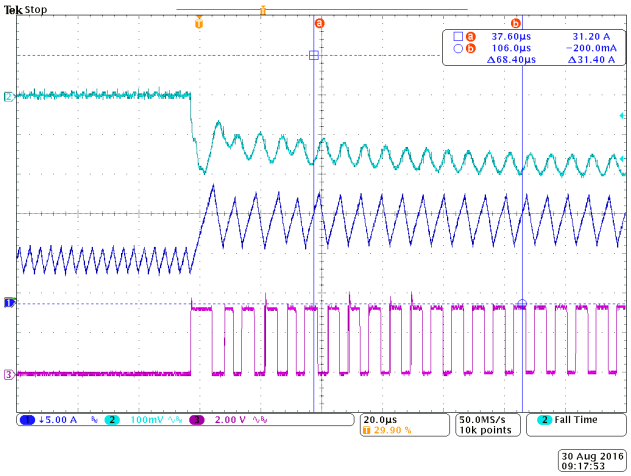

Figure 20: 50% to 100% load transient: output voltage error (light blue), inductor current (blue), NL-comparator signal output (magenta)

5. CONCLUSIONS

In this paper a combined linear and non-linear control applied to a buck converter has been presented. The proposed control is a combination of a linear control based on a conductance control principle, and a non-linear control, which intervenes only during transients. The latter is based on the detection of the output voltage variation and on the immediate application of maximum or minimum inductor current, as consequence of voltage undershoot or overshoot. Once the controlled output voltage is within the allowed range, the linear control takes back the lead of the voltage regulation.

This control technique has been applied to a buck converter, which has been bread-boarded in TEC-EP Power Laboratory. The design criteria have also been presented together with the ripple characterization.

Two different detection methods have also been designed.

Experimental results demonstrated that the proposed control technique is able to satisfy the requirements reducing the output capacitor size w.r.t. a conventional conductance control.

The effects on component stress will actually depend on the specific application, i.e. on the frequency of large load transients occurrence. If large load transients are expected to occur with high rate, then the inductance size might be reviewed w.r.t. the one used in a system with a conventional control, as it is done in the present paper.

6. REFERENCES

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