

BENEFITS AND DRAWBACKS OF A HIGH FREQUENCY GAN ZVZCPS CONVERTER

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ABSTRACT

This paper presents the benefits and drawbacks of replacing the traditional Si Mosfets transistors with enhancement mode GaN transistors in a Half-Bridge Zero Voltage and Zero Current Switching Power Switching (ZVZCPS) converter. This type of converters is usually used as Electronic Power Converters (EPC) for telecommunication satellites travelling-wave tube amplifiers (TWTAs). In this study, firstly the converter is theoretically analysed, obtaining its operation, losses and efficiency equations. From these equations, optimizations maps based on the main system parameters are obtained. These optimization maps are the key to quantify the potential benefits of GaN transistors in this type of converters. Theoretical results show that using GaN transistors, the frequency of the converter can be pushed from 125kHz to 830kHz without sacrificing the converter efficiency. This frequency increase is directly related to reduction on the EPC size and weight.

To validate the theoretical results, a 150W prototype was built and its performance measured. Experimental results show an unexpected operation at high frequencies, mainly due to the influence of the transformer parasitic capacitance and the rectifiers diodes reverse recovery effect. Finally, it can be concluded that the parasitic capacitance of the converter and the diodes recovery time are, in practice, critical parameters to increase the switching frequency keeping the ZVZCPS.

1. INTRODUCTION

In telecommunications satellites, Travelling Wave Tube Amplifiers (TWTAs) represent about 35% of the payload mass. Therefore, any improvement in its Electronic Power Converter (EPC) size and weight is critical to reduce the overall mass of the satellite. In European satellites, the EPC is usually a two-stage converter; a Buck regulator connected in series with a Zero Voltage Zero Current Power Switching (ZVZCPS) isolated high voltage converter. The ZVZCPS technique was proposed in [1] and its main advantage is that all the converter switches always operate under both Zero Voltage Switching and Zero Current Switching when Switching ON and OFF. This advantage allows achieving very high efficiencies (better than 98%) and operating at a fixed frequency with very low EMI noise generation.

The emergence of Gallium Nitride (GaN) Transistors, with lower on resistance and lower switching losses than the conventional Silicon Mosfets, and its demonstrated robustness against radiation effects, has promoted many research works focused on evaluating the benefits of this technology on power converters for aerospace applications [2-4]

This paper is focused on the potential reduction of the size and the weight of the ZVZCPS converter using GaN Transistors, increasing the switching frequency but without affecting the overall losses of the converter. Section 2 briefly describes the mathematical model of the converter, obtaining its main waveforms and the efficiency equations. In section 3 optimization maps have been developed to optimize the converter design. To validate the theoretical experimental results of a 150W prototype are presented in section 4. Finally, conclusions are presented in section 5.

2. ZVZCPS HALF-BRIDGE OPERATION

For this study, a current-fed half bridge ZVZCPS topology has been chosen. The classical current-fed push-pull topology has been discarded because, in high power European telecommunication satellites, the main bus voltage of the satellite is regulated at 100V. The EPC is supplied from the main bus, so if a push-pull topology is used, following the European Space Agency (ESA) derating standards, 250 V_{ds} transistors are needed. At the beginning of this study no commercial GaN transistors were available with this characteristic so the comparison could not be done.

In Figure 1 it is shown the ZVZCPS Half-Bridge Topology, with only two outputs for simplicity, and in Figure 2 are depicted the main waveforms of the converter.

During a period, there are four different states, named, T_{on1}, T_{gap1}, T_{on2} and T_{gap2}.

State T_{on1}: This interval starts by turning ON switch M₁ when its voltage is zero. The current through M₁ increases in a resonant manner because C_{TUN1} resonates with the leakage inductance of the main transformer, producing a sinusoidal current through M₁. The parasitic capacitance of M₂ (C_{ds2}) is charged to V_{Cun1}+V_{Cun2}

voltage and the main transformer magnetizing current (i_{Lm}) grows linearly. This interval ends when the current through the transistor M_1 is almost zero (equal to the magnetizing current).

State T_{gap1} : When the current through M_1 is almost zero (equal to the magnetizing current), switch M_1 is turned OFF. During this interval the energy stored in L_m forces the discharge of the M_2 parasitic capacitance (C_{ds2}), charging the M_1 parasitic capacitance (C_{ds1}) linearly at a constant current. During this interval there is no transfer of energy from the input to the output and all the diodes are OFF. The tuning capacitors C_{tun1} and C_{tun2} are linearly charged with the input current of the converter I_{in} .

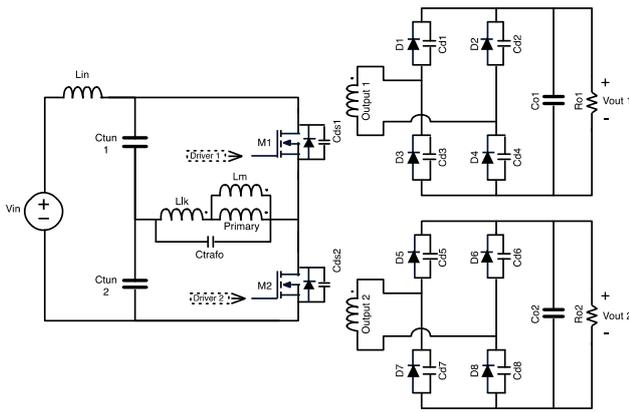


Figure 1. Two output Half-Bridge ZVZCPS Converter

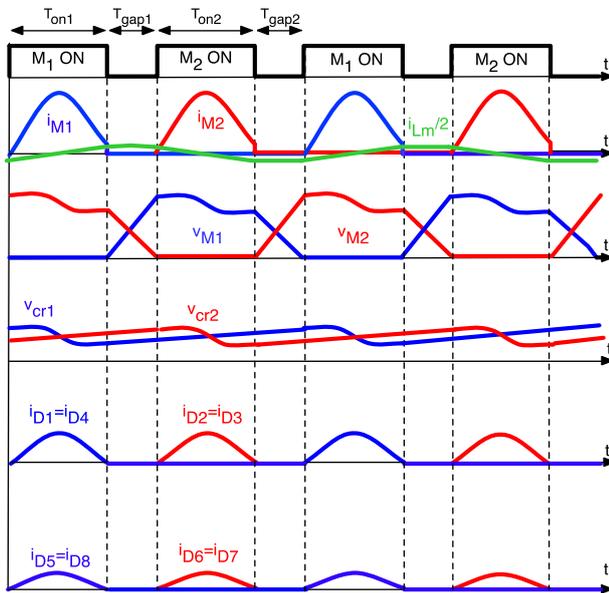


Figure 2. Two output Half-Bridge ZVZCPS Converter main waveforms

Intervals T_{on2} and T_{gap2} are analogous to interval T_{on1} and T_{gap1} respectively. In state T_{on2} , switch M_2 is turned ON and the parasitic capacitance of M_1 (C_{ds1}) is charged to

$V_{Ctun1} + V_{Ctun2}$. During interval T_{gap2} The energy stored in L_m forces to discharge the M_1 parasitic capacitance (C_{ds1}), charging the M_2 parasitic capacitance (C_{ds2}).

In order to optimize efficiency of the designed converter, all the converter power losses equations have been calculated.

2.1 Transistor Losses

Conduction Losses: The transistor conduction losses are directly related with the RMS current flowing through them and their ON resistance. To be more accurate the magnetizing current is also used in this calculus. The magnetizing current during the ON time has a quasi-triangular shape so its RMS value can be easily calculated:

$$P_{Mos} = 2I_{Mos(RMS)}^2 R_{ds} + I_{Lm(RMS)}^2 R_{ds} \quad (1)$$

Switching Losses: Although the converter has been described as it always commutates at Zero Voltage and Zero Current and there are not switching losses, this is not really true. When the transistor is turned off, the magnetizing current is flowing through it. To calculate these losses, the voltage of the transistor during the OFF commutation (V_{off}) has been simplified to the voltage of the parasitic capacitance being charged at a constant current I_{Lm} during the time that the switch last to be turned off (T_{off}).

$$V_{off} = \frac{T_{off} I_{Lm}}{C_{eff}} \quad (2)$$

$$P_{off} = 2 (0.5 V_{off} I_{Lm} T_{off} F_{sw}) \quad (3)$$

Driver Losses: Driver losses have to be considered in both transistors and they are calculated multiplying the energy provided to the transistor gate by the switching frequency.

$$P_{gate} = 2(V_{drv} Q_{gate} F_{sw}) \quad (4)$$

2.2 Diode Losses

The current flowing through the diodes is proportional to the transistors multiplied by the transformer turn relation ratio.

$$P_D = 4I_{Dsec1(AVG)} \cdot V_{FDsec1} + 4I_{Dsec2(AVG)} \cdot V_{FDsec2} \quad (5)$$

2.3 Tuning Capacitors Losses

The losses are the ones associated to the equivalent serial resistance (ESR) of the capacitors:

$$P_{CTun(RMS)} = 2I_{CTun(RMS)}^2 \cdot ESR_{CTun} \quad (6)$$

2.4 Output Capacitors Losses

As in the previous case, losses are associated to the equivalent serial resistance (ESR) of the output capacitors:

$$P_{Co} = I_{Co1(RMS)}^2 \cdot ESR_{Co1} + I_{Co2(RMS)}^2 \cdot ESR_{Co2} \quad (7)$$

2.5 Transformer losses

Core Losses: For the calculations, it is used the equation provided by Ferroxcube in the application note "Planar Transformed Design" [5]. Core losses are calculated as function of frequency (f in Hz), peak flux density (B_{peak} in T) and the temperature (T in °C)

$$P_{core} = C_m f^x B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \quad (8)$$

In this formula, C_m , x , y , ct_0 , ct_1 and ct_2 are parameters which have been found by curve fitting of the measured power loss data. These parameters are specific for a ferrite material and can be found in the Ferroxcube application note.

Copper Losses: Copper losses are the ones produced by the current in the conductors of the transformer windings due to their associated resistance.

$$P_{cu} = \frac{\rho (MLT) n_1^2 I_{tot(RMS)}^2}{W_A K_u} \quad (9)$$

Where: ρ is the wire effective resistivity, MLT is the mean length of the transformer turns, n_1 is the number of turns in the primary, $I_{tot(RMS)}$ is the sum of the rms winding currents referred to the primary, W_A is the window area of the core and K_u is the window utilization factor, usually 0.1878 for planar transformers.

The minimum number of turns (n_1) is defined by the maximum peak flux density allowed to limit the core losses of the transformer.

$$n_1 \geq \frac{V_{in} T_{ON}}{2 \cdot B_{peak} \cdot A_e} \quad (10)$$

3. ZVZCPS HALF-BRIDGE OPTIMIZATION MAPS

From the converter losses equations derived in previous section, a graphic representation of the converter losses and efficiency can be obtained. These graphic representations have been called "Optimization Maps" where all the losses and the efficiency are represented as function of the transistors ON time (T_{ON}) and the magnetizing inductance of the transformer (L_m). These parameters have been chosen because the whole converter design depends only on the value of these two parameters. These optimization maps are the key to quantify the potential benefits of GaN transistors in this type of converters.

The comparison has been done for a 150W 50V converter with two 75W outputs (250V and 500V). Two converters have been designed from these specifications, a Si converter operating at a frequency of about 125kHz and a GaN converter operating at a frequency of about 1MHz. For the Si converter the transistors chosen are RJK1056DPB from Renesas Technology and the diodes are MUR130 for the 250V output and the MUR160 for the 500V output. For the GaN converter the transistors are EPC2001 from EPC and the diodes are the same as in the Si converter. It is important to emphasize that, although the GaN transistor have better characteristics than the Si ones, their drain-source parasitic capacitance is of the same order or even higher than in Si transistors. This is one of the major drawback for pushing up the frequency using GaN transistors in this type of resonant converters, because during the GAP time this capacitance have to be charged/discharged as it was explained in section 2.

The transformer has been designed with the restriction that its maximum core losses should be less than the 0.25% of the converter power (325mW). From this restriction the maximum peak flux density is calculated, and once the maximum B_{peak} is fixed, the core material, dimensions and the number of turns are calculated. For this study the cores needed are: E43+PLT43 (material 3F3) with 5 turns in the primary side for the Si design and E32+PLT32 (material 3F3) with 3 turns in the primary side for the GaN design.

The final size and weight of the designed EPC converters are: 225 cm² / 397g for the Si one and 121 cm² / 198g for the GaN one.

The optimization maps obtained for the Si and GaN designs are depicted in Figure 3. In each map the centre of the overlapped circle shows the chosen operating point for the comparison ($T_{on}=4\mu s$, $L_m=50\mu H$, Freq=125kHz in the Si Converter and $T_{on}=0.5\mu s$, $L_m=3.1\mu H$, Freq=830kHz in the GaN Converter). In both designs the converter theoretical efficiency is the same, 98.25%.

From the optimization maps can be deduced that transistor losses are lower as the switching frequency decreases (higher T_{on}). This is due to the fact that both, the switching losses and the driver losses are directly proportional to the switching frequency. Besides, it can be observed the trend to increase losses with the reduction of L_m . This is because a reduction of L_m involves a higher magnetizing current and then also higher switching losses.

In the transformer losses maps, it can be observed that the trends in both designs are different. This is mainly produced by the frequency limits of the core material (3F3). In the the GaN design, working at 830kHz, this material is very near to its frequency limit.

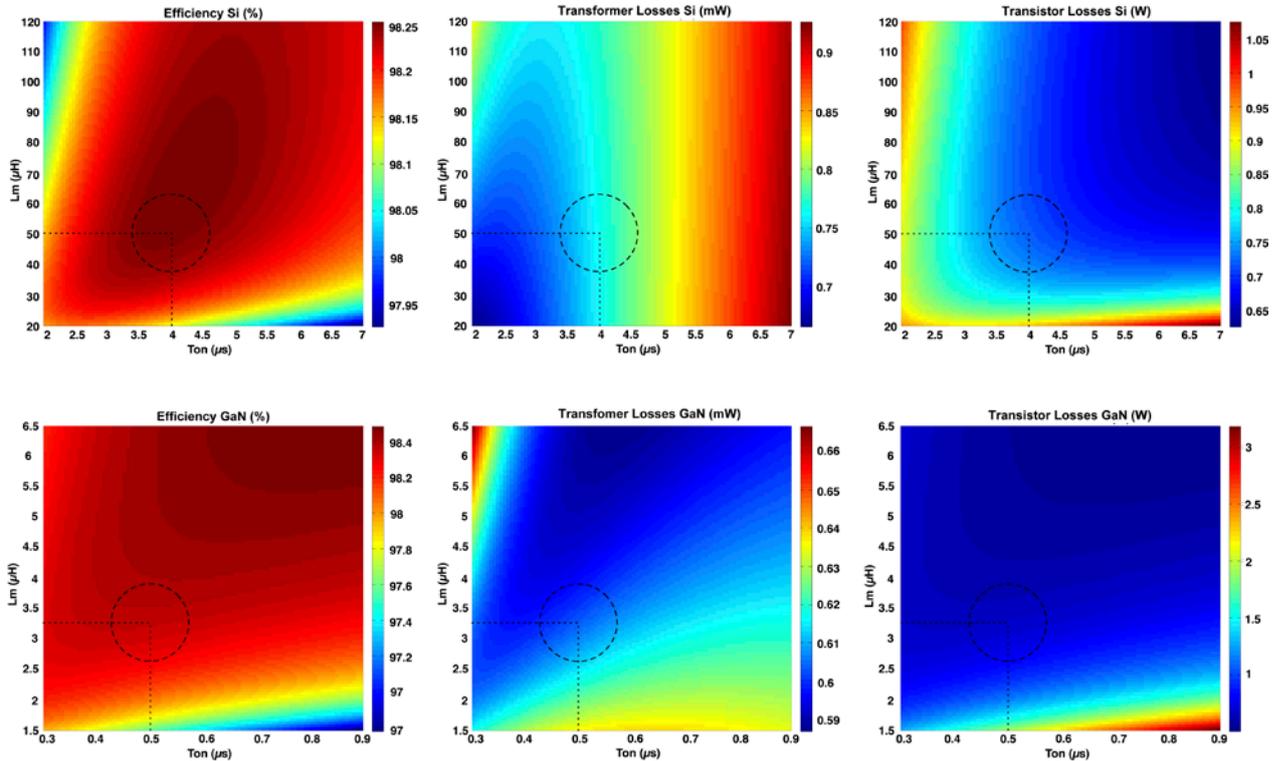


Figure 3. Optimization Maps.

x-axis variable: Transistors ON time, *y*-axis variable: Transformer Magnetizing Inductance.

Finally, in the efficiency maps it can be observed that none of the converters are working at the maximum efficiency point, maximum efficiency can be achieved decreasing the switching frequency but increasing the size and the weight of the converter. Efficiency higher than 98% has been fixed as target for the comparison. As can be seen, this efficiency can be achieved using GaN transistors switching at a frequency of 830kHz, about seven times higher than the frequency used with the traditional Si transistors (125 kHz).

4. EXPERIMENTAL PROTOTYPE

A 150W experimental prototype was implemented to validate the theoretical results. The desired control signals were generated with an astable 4017 and an LM5113 GaN driver from Texas Instruments was used to switch the GaN transistors.

Initially, a planar transformer was designed and implemented. The core used was E32+PLT32 (material 3F3) with 3 turns in the primary side, 30 turns in one secondary and 60 turns in the other one. The secondaries were implemented in a 16-layer PCB and the primary was implemented using three turns of copper foil. Once implemented, the transformer was measured and characterized, dealing in a parasitic capacitance of 34nF. This parasitic capacitance is too high for a ZVZCPs converter working at 830kHz. It is worth noting that the

total parasitic capacitance of the converter must be charged/discharged during the GAP time, using the energy stored in the magnetizing inductors, so if the parasitic capacitance is too high it is needed an increment of the GAP time (reducing the frequency) or an increment of the magnetizing current (incrementing the losses). In figure 4 it is shown the experimental prototype with the planar transformer.

A second transformer was implemented on a RM14 core (material N49) with 3 turns in the primary and 30 and 60 turns in the secondaries. Its magnetizing inductance was adjusted to 3 μ H and the measured parasitic capacitance was 1.32nF. This value is more appropriate for the converter so this transformer was the one used for the experimental tests.

In figure 5 it is shown an oscilloscope screenshot with the main converter waveforms. As can be seen, the experimental waveforms do not match with the theoretical ones during the GAP time. The current through the primary of the transformer is not null, it has a sinusoidal shape, even changing its polarity. This is due to rectifiers diodes reverse recovery effect, when the diodes are switched off, the reverse current is reflected in the primary side, even cancelling the magnetizing current and requiring the body-diode of the transistor to conduct. This effect has been magnified at high frequencies due to

the higher rate of change of the diode current during the ON time, dealing in a higher reverse current. This effect has been neglected in the theoretical studies because at low frequencies is almost null. In further researches it will be interesting to study the influence of the recovery time in the overall behaviour of the converter.

Although the converter is not working as it is desired, the efficiency have been measured with a High Performance Power Analyzer WT1800 from Yokowaga. The measured efficiency is presented in figure 6, this efficiency includes the auxiliary power supply used to power the control part of the converter. At full load (150W) the efficiency is 90.7%, quite lower than the one theoretical calculated. This is due to the fact that the final transformer core is not the same that the one used for the calculations, the auxiliary power supply consumption and the most important reason the behaviour of the prototype during the GAP time.



Figure 4. 150W Half-Bridge ZVZCPS Prototype

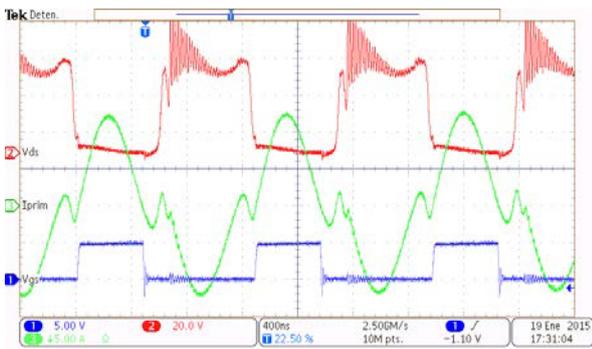


Figure 5. 150W ZVZCPS Prototype waveform
 Red – Drain-Source Voltage, Green – Primary Current,
 Blue – Transistor driving signal.

5. CONCLUSIONS

GaN transistors have lot of advantages compared with their Silicon counterparts. They have lower conduction and switching losses, so it is possible to design more efficiency converters or to increase the frequency of the actual converters reducing it size and weight. In the case of ZVZCPS converters, the GaN transistors

benefits is limited because this type of converters has very high efficiency with very low commutation losses.

Besides, increasing the switching frequency is limited by all the parasitic capacitance of the converter. Planar transformers are also a promising technology to reduce the size of the converters but they have a very high parasitic capacitance so its benefits in this type of converters is also reduced. Besides, when the switching frequency it is increased, the diodes reverse recovery effect is magnified, affecting the original converter behaviour.

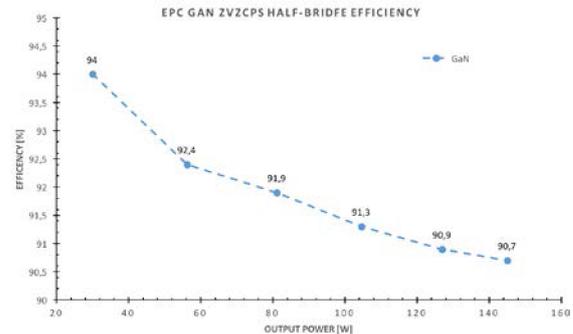


Figure 6. 150W ZVZCPS prototype measured efficiency

6. ACKNOWLEDGMENTS

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