A STUDY OF A B^{3}R CONVERTER BASED PCU, TO CONFIRM THE FLEXIBILITY AND PERFORMANCE OF THE CONVERTER TOPOLOGY

Erik Mache [(1)], Michael Koch [(2)]

[(1)] *ASP Equipment GmbH, Am Wasserstall 2, 88682 Salem, Germany, Email: e.mache@asp-equipment.de*
[(2)] *ASP Equipment GmbH, Am Wasserstall 2, 88682 Salem, Germany, Email: m.koch@asp-equipment.de*

ABSTRACT

The main objective of this activity was to study the B^{3}R converter [1] and to confirm its flexibility and performance (mainly efficiency and mass reduction) versus solutions that is implemented in a satellite PCU. For details see [2] ESTEC SOW.
An architecture with centralised regulated bus, single battery and centralised solar array was selected for this study.
Project Plan:
- Study, design and development of an evaluation prototype, based on the B³R topology (including protections and control loops).
- Study, design and development of an Electrical Elegant Breadboard including three power stages, based on the B³R topology (including protections and control loops).
- Laboratory tests of these converters (power stages, control loops and protections).
- Conclude the study by comparing the achieved performances (including efficiency and mass) versus current solutions implemented on a satellite PCU. Summary of the pros and cons of the use of the B^{3}R concept.

1. INTRODUCTION

In a satellite, the main function of a Power Conditioning Unit (PCU) is to manage the energy coming from several power sources (usually solar arrays and battery) and to deliver it continuously to the users in an appropriate form during the overall mission.
The ESA Power Conditioning Department proposed new solutions based on Buck Buck Boost Regulators (B³R), which appeared to be a promising alternative [1]. They predicted on one hand more efficient regulators and or on the other hand a better utilisation of the source, since they are capable of operating on a wider range of source characteristics. This new B³R topology is a multiple port DC DC converter, which can interface a solar array, a battery and generate a regulated DC bus voltage.
The B^{3}R topology is a flexible topology that can be used in different architectures for different applications.

For this study different architectures of the solar array (centralised or distributed), the regulated bus (centralised or multiple) and the battery (single or segregated) were discovered. After a comparison of properties, the architecture "Centralised Regulated Bus and Single Battery and Centralised Solar Array" was selected.

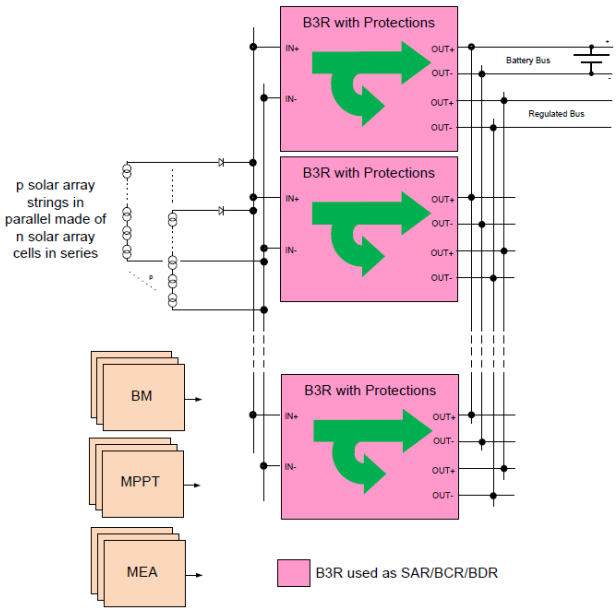

Figure 1-1: Centralised Regulated Bus and Single Battery and Centralised Solar Array

2. STUDY LOGIC

The objective of this task was to design and build an Electrical Elegant Breadboard to study the adequacy of the protections and evaluate the stage performances at B³R level and at architecture level.
According to the selected architecture an Electrical Elegant Breadboard (EEBB) of the single point failure free architecture was designed. Since the design was suitable the Agency decided to approve it.
The power architecture contains three B³R power stages with their dedicated current control loops and protections. The higher level control loops are located on a separate printed circuit board.
For the purpose of the study it was found as adequate to manufacture the Electrical Elegant Breadboard with commercial EEE parts, having same or equivalent functionalities and performances as Hi-Rel EEE-parts..

3. DESIGN DESCRIPTION

The EEBB is built up on two circuit boards and one mechanical frame. One board is the Power Board (blue in Fig. 3-1). It includes three B^{3}R power stages. The Controller Board (green in Fig 3-1) contains the high level controller which is designed to be single point failure free. The following figure shows the internal signal routing of the EEBB and the external connections.

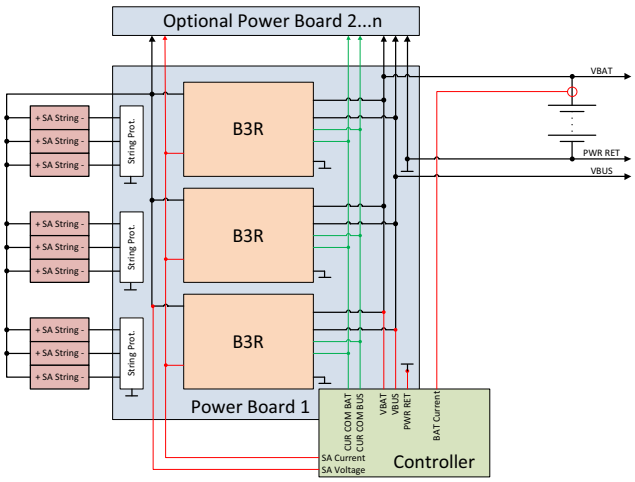

Figure 3-1: EEBB Block Diagram

3.1. B^{3}R Power Stage

The B^{3}R power stage is a three port DC/DC converter. Solar Array (SA) input is passed via a buck/boost stage to charge the battery and supply the bus. Both SA input switches (buck/boost) are controlled by a battery port output current controller. The regulated bus output is supplied by a buck stage, with the buck switch controlled by an bus port output current controller. The power stage can operate in three different operating modes:

- BUCK (SA Voltage > Battery Voltage)
- Direct Energy Transfer (DET) (SA Voltage = Battery Voltage)
- Boost (SA Voltage < Battery Voltage)

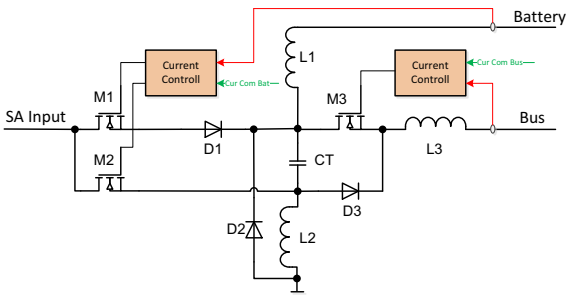

Figure 3-2: B^{3}R Power Stage

3.2. Protection

Every B^{3}R power stage protection has an independent circuit which monitors several signals. Three MOSFET switches are controlled by the protection to isolate the power stage in case of a detected failure (battery protection switch, solar array protection switch and protection switch against short circuit to ground).

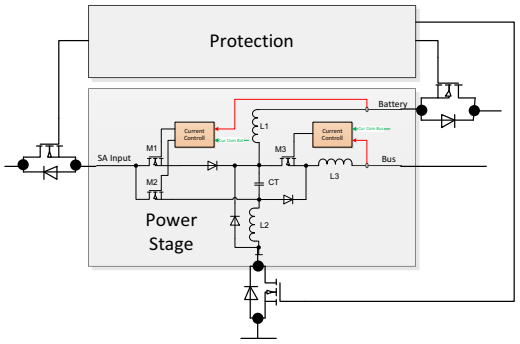

Figure 3-3: Protection Scheme

The switches are controlled by a central latch. When an over load condition is detected, the latch is set, the power stage is disabled and the protection switches opens. The latch stays active until a power cycle occurs (SA and Battery disconnect and reconnect) or an external RESET command is issued. Fig. 3-1 shows the possible sources to set and reset the latch, and the state of the protection switches and the power stage.

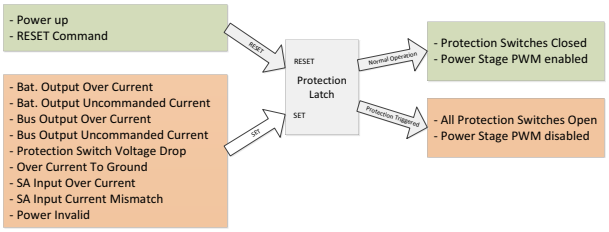

Figure 3-4: Protection Latch

3.2.1. Battery Output Over Current

A segregated current sense amplifier is connected to the shunt resistor in the battery port output. If the charge current to the battery exceeds the limit, the protection will be triggered. This threshold is set around to 14A, which is well above the maximum current that the control circuit in normal operation will permit (10A). Buck and boost PWM signals are disabled when the protections trigger.

3.2.2. Battery Output Uncommanded Current

The current sensed by the battery over current protection is used to detect uncommanded current to the battery. The current command signal from the controller

board is used to detect a zero current command. If a zero current command is detected and there is still current flowing on the battery port, the protection will be triggered. The threshold to detect uncommanded current is 0,5A.

3.2.3. Bus Output Over Current

A segregated current sense amplifier is connected to the shunt resistor in the battery port output. If the charge current to the battery exceeds the limit, the protection will be triggered. This threshold is set around to 9A, which is well above the maximum current that the control circuit in normal operation will permit (7,6A). Buck PWM signals are disabled when the protection trigger.

3.2.4. Bus Output Uncommanded Current

The current sensed by the bus over current protection is used to detect uncommanded current to the bus. The current command signal from the controller board is used to detect a zero current command. If a zero current command is detected and there is still current flowing on the bus port, the protection will be triggered. The threshold to detect uncommanded current is 0,5A.

3.2.5. Protection Switch Voltage Drop

In normal operation, the voltage drop on all three protection switches is monitored. The voltage drop is caused by the RDSon and the current of the protection switch. If a protection switch fails in a way that increases RDSon, the voltage drop will also increase. A voltage drop over 0,7V will trigger the protection latch.

3.2.6. Over Current to Ground

In the normal operating the current through Ground can flow in both directions. This depends on the operating condition. In a failure case, the current flows to ground. To protect from a short circuit to ground in any point of the power stage, the current to ground is sensed. If the current increases over the threshold, the protection will trigger.

3.2.7. SA Input Over-Current

The SA input current will be measured using the voltage drop over the input filter inductor. If the current increases the max input current threshold, the protection will trigger.

3.2.8. SA Input Current Mismatch

Fig. 3-5 shows the connection principle between the different power stages. The SA input current will be measured using the voltage drop over the input filter inductor. The current is compared to the input current of another power stage. In normal operation all B3R power stages get a common current output command. Therefore the output currents are identical. Then also the input currents are identical. If one power stage suffer a failure which increase the power dissipation of that converter, the input current will increase to maintain the commanded output current. This will be detected by the SA input current mismatch monitor and triggers the protection latch.

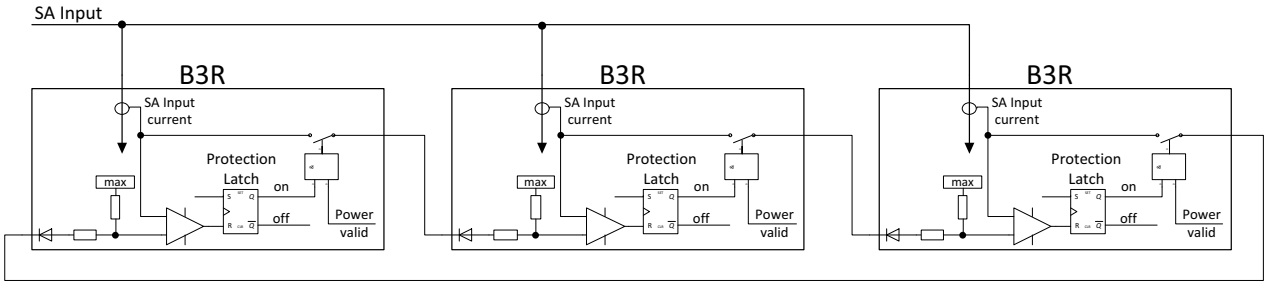

Figure 3-5: SA Input Current Mismatch Monitor

This monitor is combined with the input over current protection. The threshold to activate the protection is either the max input current, or a reduced level transmitted from another power stage. The power stage itself transmits its input current level to the next power stage for comparison. To avoid unintended trigger of that monitor, a current level will only be transmitted if the power stage operates in normal conditions. An activation of the protection latch or an internal supply failure disables the transmission of the input current level to the next stage.

3.2.9. Solar Array Short Circuit Protection

In addition, there are several input protection switches connected in the return line of the solar array that will isolate shorted strings of the solar array avoiding losing the whole section or solar array. As a baseline, 3 switches (MFETs) per B3R are implemented.

If a failure in the solar array side, for example in the driving mechanism, leads to a short circuit of it, and all the sections are directly connected together, as happens to be in a centralised solar array, the whole solar array

will be lost. However, if the solar array is divided in sections, each one connected through a protection switch, in case one fails, only that section will be lost, minimising in this way the risk.

3.3. Control Scheme and MPP Tracking

The control of the PCU is implemented with different control loops.

- Basic current control loops on the power stage
- High level control loops on the controller board

3.3.1. Basic Current Control Loops

The basic current control loops are located on the B^{3}R power board and regulates the output current of the battery port and the bus port. Fig. 3-6 shows the two basic current control loops which get the current command from the high level controller fitted on the control board. These basic current control loops are implemented on each B^{3}R power stage. This arrangement ensures equivalent current sharing over the different power stages. The output of the current controllers is feed to a voltage comparator. It is compared to a saw tooth signal to generate a PWM signal which drives the power stage. To insure proper start up the controller is initialised by the protection latch. With an active protection signal, the integrator of the controller is held in reset state. When the converter gets enabled (power up or enable command) the controller does a soft start.

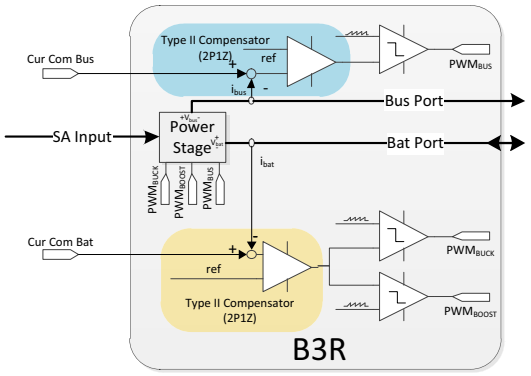

Figure 3-6: Basic Current Control Loops

The power stage for the battery output supports buck and boost operation. Two separate comparators are used to generate the PWM signals for the boost and buck switch. The offset of the two saw tooth signals for buck and boost mode is arranged at different voltage levels. This ensures segregated operation modes dependant on the SA and battery voltages. Boost mode for SA voltage lower battery voltage. Direct energy transfer (DET) for SA voltage equal battery voltage. Buck mode for SA voltage higher battery voltage. The output voltage of the current controller determines the operating mode.

3.3.2. High Level control loops and MPP Tracking

The high level controller generates the current command for the basic control loops. These current command signals are global signals for all B^{3}R power stages. To reach the required system availability they have to be single point failure free. Therefore these signals are generated by majority voted outputs of the triplex controllers.

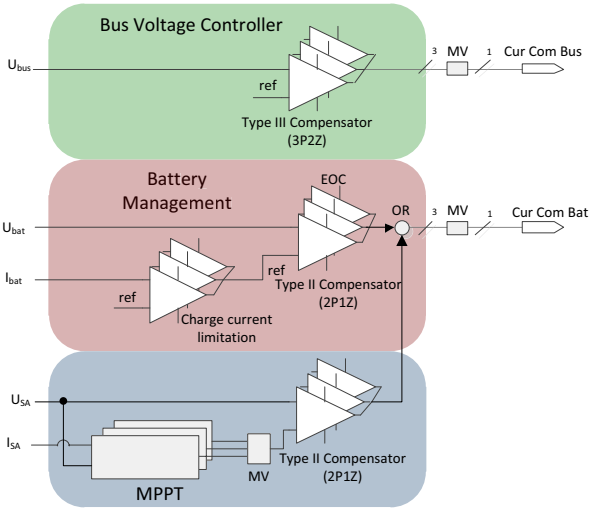

Figure 3-7: High Level Control

3.3.3. Bus Output Voltage Controller

The bus voltage controller is a Type III compensator. It provides three poles and two zeros, which are selected to reach the desired gain and phase margin. The compensator is implemented three times with a following majority voter. The voted output is the current command for the bus output and is distributed to all converters. See Fig. 3-7.

3.3.4. End of charge control Loop

This loop control limits the maximum battery charge voltage and current. It contains two compensators. One is a type II compensator to control the battery charge voltage, the other is a type I compensator which controls the max charge current. The schema is shown in Fig. 3-7, Battery Management. The battery voltage controller has a max voltage reference which can be reduced by the max charge current controller. This arrangement ensures compliance with the battery operating limitations. The output of the battery management controller is linked together with the output of the MPPT. The lowest current command will generate the current command for the battery output.

3.3.5. MPP Tracking

The maximum power point tracker uses the "perturb and observe" method to find and track the maximum power point. Three independent trackers generate a voted SA voltage reference. A SA voltage controller uses this reference to generate a battery output current command. See Fig. 3-7 for the schema. The SA voltage controller is implemented with a type II compensator which provides two poles and one zero. They are positioned in a way to reach the desired phase and gain margin.

4. TEST RESULTS

The B3R module was tested in all operating modes (Buck / DET / Boost / Charge / Discharge / MPPT / Battery management) and behaves as expected. This includes stability measurements (small signals and large signal transient), efficiency measurements (including control consumption and protections dissipation), power stages waveforms measurements, transient measurements from MPPT mode to Charge mode (and the opposite), transient measurements between Buck/Boost modes, and DET mode.

4.1. Efficiency

Efficiency was measured on the connectors of the EEBB and based on one power stage. It includes all internal B3R losses like the cooper tracks, filter inductors, protection switches and current sense shunts, auxiliary power supply and the power stage. The following figures show the efficiency for different operating modes with different load and charge current. The X-axis shows the battery port current. Negative current means battery discharging. The Y-axis shows the bus current.

	-3	-2	-1	0	1	2	3
5	94,5	92,8	91,2	89,5	88,9	88,4	87,8
4		93,6	91,9	89,9	89,5	89,1	88,7
3			92,7	90,3	90	89,8	89,5
2				87,5	88,4	89,3	90,3
1				84,7	86,8	88,9	91

Figure 4-1: Boost Mode (VSA=25V, VBAT=42V, VBUS=28V)

	-3	-2	-1	0	1	2	3	4	5	6	7
5	94,8	93,7	92,7	91,6	91,7	91,8	91,9	91,8	91,6	91,5	91,3
4		94,2	92,8	91,5	91,7	92	92,2	92	91,9	91,7	91,6
3		94,6	93	91,4	91,8	92,1	92,5	92,3	92,2	92	91,8
2				89,4	90,5	91,6	92,8	92,6	92,5	92,3	92,2
1				87,4	89,3	91,1	93	92,9	92,8	92,6	92,5

Figure 4-2:Buck Mode (VSA=42V, VBAT=31V, VBUS=28V)

	-3	-2	-1	0	1	2	3	4	5	6	7
5	95	94,4	93,9	93,3	93,5	93,6	93,8	93,6	93,4	93,1	92,9
4		94,3	93,9	93,5	93,7	94	94,3	94	93,8	93,5	93,3
3		94,2	93,9	93,6	94	94,3	94,7	94,4	94,2	93,9	93,6
2				91,8	92,8	93,9	94,9	94,6	94,4	94,1	93,9
1				90	91,7	93,4	95,1	94,9	94,6	94,4	94,1

Figure 4-3: DET Mode (VSA=VBAT=40V, VBUS=28V)

4.2. Stability Of The Control Loops

In battery charging mode, the MPPT ensures always operating in MPP. If the charging voltage of the battery is reached, the power, delivered by the SA, has to be reduced. There are two different regions to operate the SA, to reduce the power of the SA: Current region and voltage region.

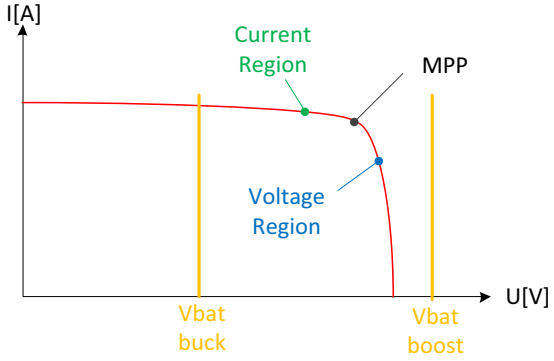

Figure 4-4: SA EOC Operating Modes

4.2.1. Stability EOC In Voltage Region

To operate the EOC in the voltage region of the SA, the current control loop is configured to operate in voltage region. Therefore the pulse wide of the power switches will be reduced, when a lower output current is demanded. Zero current demand cause the buck and boost switches to open, leading to the maximum no load voltage of the SA. All loops were measured and analysed.

The current loops were measured in boost and buck operation and reach all a phase margin > 60° and gain margin > 10 dB with a bandwidth > 17 kHz.

The input voltage loops result where measured in buck and boost operation and reach all a phase margin > 56° and gain margin > 10 dB with a bandwidth > 1,6 kHz.

4.2.2. Stability EOC In Current Region

To operate the EOC in the current region of the SA, the current control loop is configured to operate in current region. Therefore the pulse wide of the power switches will be increased, when a lower output current is demanded. Zero current demand cause the buck and boost switches to close, leading to the maximum short current of the SA. All loops were measured and analysed.

The current loops were measured in boost and buck operation and reach all a phase margin > 60° and gain margin > 10 dB with a bandwidth > 400 Hz.

The input voltage loops result where measured in buck and boost operation and reach all a phase margin > 49° and gain margin > 11 dB with a bandwidth > 1 kHz.

The result shows stable operation in every condition. The bandwidth is much lower compared to operating in

the voltage mode. Further investigation showed the limiting factor is the capacitance on the SA input. In the current region, the SA behaves as a current source for low frequencies (high impedance). As frequency increase the SA behaviour turns to a voltage source (low impedance).

4.3. Internal Failures Stimulation

To verify the detection of power component failures all cases, which are identified to be critical, were stimulated by HW failure injection. The critical failure cases where identified by analysis and simulation and a result of the FMECA.

All tests where done in the following way:

- Applying the failure during normal operation and record the reaction.
- With the failure still applied, enable the converter by an enable command and verify the reaction of the protection.
- Remove the failure stimulation and enable the converter by an enable command.

M2 SD short boost/buck

- OVER CURRENT TO GROUND

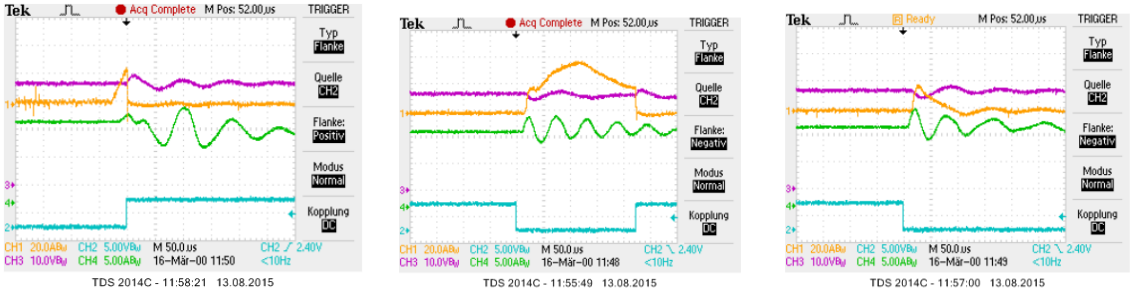

Figure 4-5: M2 SD Short Stimulation

CH1: Ground Cur, CH2: prot. Latch, CH3: Bat Voltage, CH4: SA Current

M2 DG short boost/buck

- SA INPUT CURRENT MISMATCH

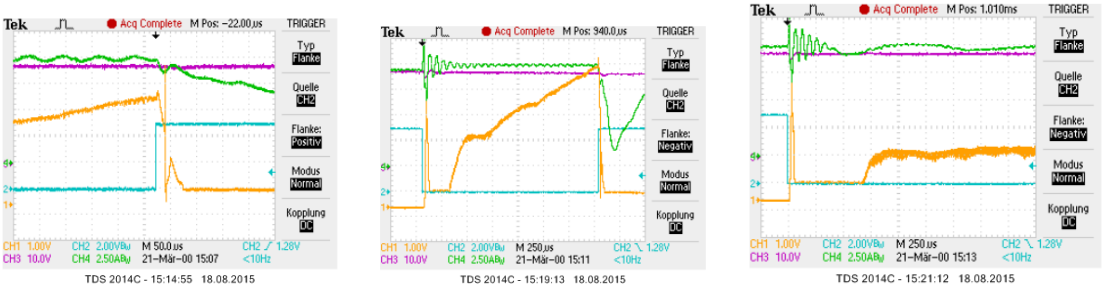

Figure 4-6: M2 DG Short Stimulation

CH1: Converter input current, CH2: prot. Latch, CH3: Bat Voltage, CH4: SA Current

M1 SD short buck

- SA INPUT CURRENT MISMATCH

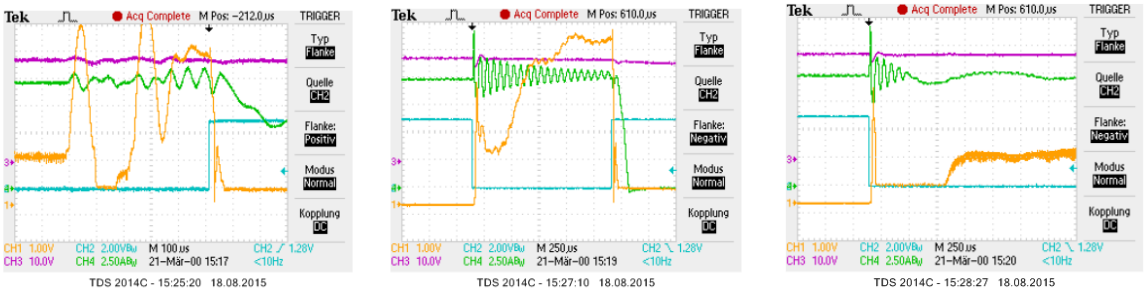

Figure 4-7: T3 M1 Short Stimulation

CH1: Converter input current, CH2: prot. Latch, CH3: Bat Voltage, CH4: SA Current

D2 open buck

- SA INPUT CURRENT MISMATCH

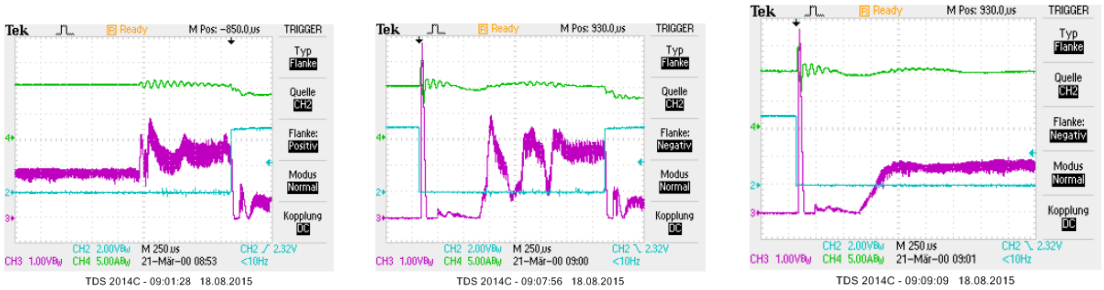

Figure 4-11: D2 open Stimulation

CH2: prot. Latch, CH3: Converter input current, CH4: SA Current

D2 short buck/boost/eclipse

- OVER CURRENT TO GROUND

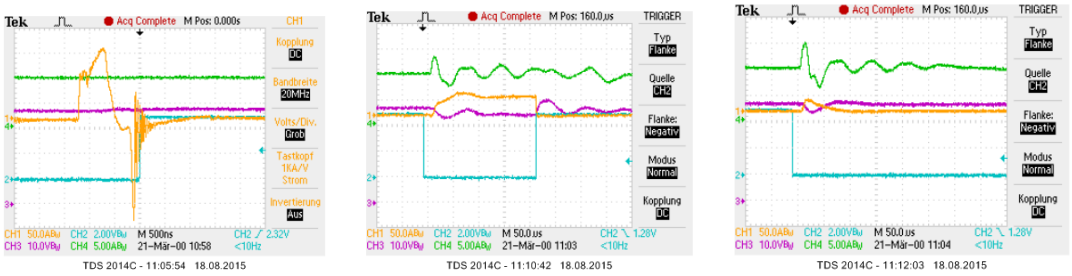

Figure 4-8: D2 short Stimulation

CH1: Ground Cur, CH2: prot. Latch, CH3: Bat Voltage, CH4: SA Current

D3 open buck/boost/eclipse

- SA INPUT CURRENT MISMATCH

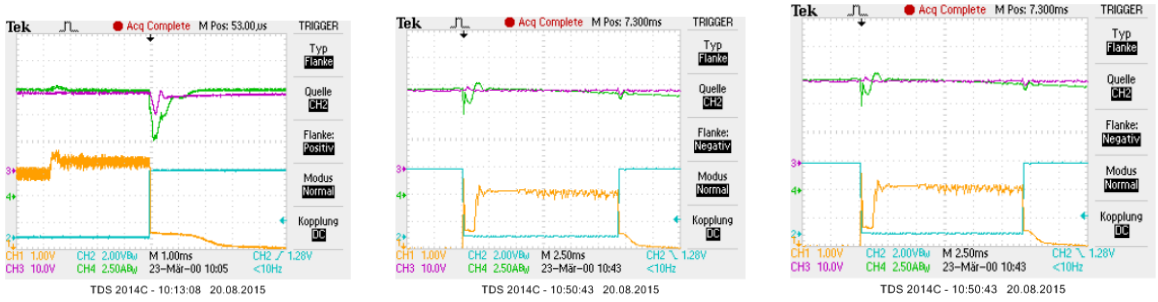

Figure 4-9: D2 open Stimulation

CH1: Converter input current, CH2: prot. Latch CH3: Bus Voltage, CH4: SA Current

D1 short boost

- OVER CURRENT TO GROUND

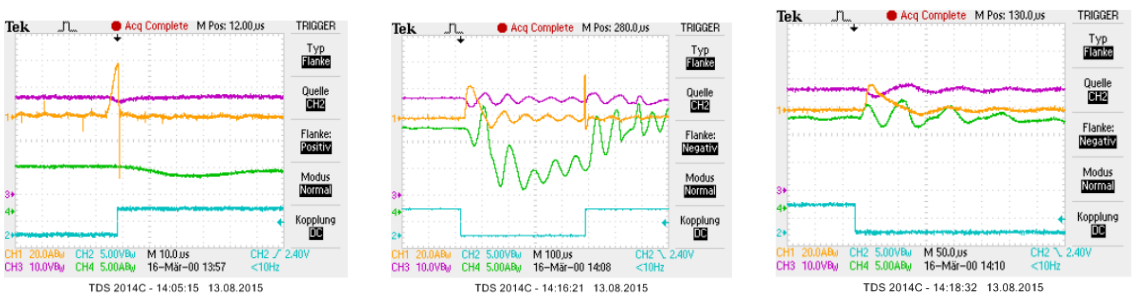

Figure 4-10: D1 A1 short Stimulation

CH1: Ground Cur, CH2: prot. Latch, CH3: Bat Voltage, CH4: SA Current

5. EEBB HARDWARE

Picture 3 shows the EEBB hardware. The three power stages can be identified on the power board mounted in the frame within three vertical sections. The Controller Board is assembled above the Power Board.

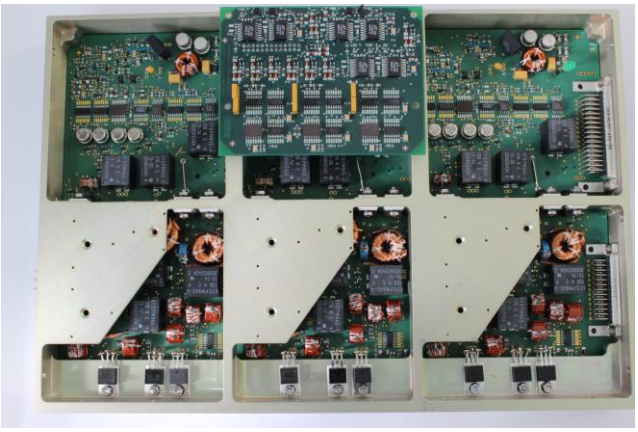

Figure 5-1: EEBB Hardware Top View

6. ACTIVIES DURING THE STUDY

- Study, design and develop of an evaluation prototype, based on the B³R topology (including protections and control loops).
- Study, design and develop of an Electrical Elegant Breadboard including three power stages, based on the B³R topology (including protections and control loops).
- Test in laboratory environment (power stages, control loops and protections).
- Concluding the study by comparing the achieved performances (including efficiency and mass) versus current solutions implemented on a satellite PCU. Summary of pros and cons of the use of the B³R concept.

The B3R module was tested in all operating modes (Buck / DET / Boost / Charge / Discharge / MPPT / Battery management) and behaves as expected.
This includes:

- Stability measurements (small signals and large signal transient).
- Efficiency measurements (including control consumption and protections dissipation).
- Power stages waveforms measurements.
- Transient measurements from MPPT mode to Charge mode (and the opposite).
- Transient measurements between Buck/Boost modes, and DET mode.

7. SUMMARY OF THE STUDY RESULTS

As a result of this activity, it was shown that a flexible PCU with several B³R power stages can be implemented. For the comparison with current implementations the following key parameters were determined:

- SA input voltage: 0 – 60V
- Battery Voltage: 32 – 50V
- Regulated Bus Voltage: 28V
- Maximum solar array input power of one power stage: 600W
- Efficiency in buck mode, including supply and protections: 93% max.
- Efficiency in boost mode, including supply and protections: 91% max.
- Weight-Power ration in a two out of three operating condition: 1.725g/W (worst case)
- Weight-Power ration in a five out of six operating condition: 1.38g/W

A PCU implementation of a single point failure tolerant B³R topology was successfully demonstrated. In a primary PCU, single point failure tolerance is essential for the operation in a spacecraft. It was found as important to detect and isolate failures in the power stage. This ensures that after a failure case neither the Solar Array, the Battery and the Bus ports are shorted, nor significant power dissipation will propagate heat and damage redundant power stages. Detailed analysis and tests with stimulated power components failures where done and showed a reliable detection and isolation of the affected power stage.
Operating during end of charge (EOC) in the current or voltage region of the Solar Array was tested. It was shown that both operation modes are feasible with different characteristics.
Also it was shown, that the B^3R is able to handle abnormal conditions, like start up from depleted battery.

8. REFERENCES

1. Buck-Buck-Boost Regulator (B^3R) for Spacecraft Power Conditioning Unit, O. Mourra, A. Fernández, S. Landstroem & F. Tonicello, Proceedings of the 9th European Space Power Conference, 2011, Saint Raphael, France.
2. ARTES 5.1 Statement of Work PCU module based on Buck Buck Boost Regulator (B^3R) Reference nr.: 12.1TT.56 Technical Officer: Olivier Mourra, ESTEC, Noordwijk