INTERLEAVED, MULTI-SWITCH, MULTI-PHASE BOOST CONVERTER FOR BATTERY DISCHARGE REGULATORS

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ABSTRACT

Non-isolated step-up voltage converters are commonly required as Battery Discharge Regulators (BDR's). The Weinberg and boost derived topologies are traditionally employed in modules up to one or two kilowatts. The Interleaved Boost Converter (IBC) is a distributed power processing approach that provides some advantages: reduced power processing (current) per phase, distributed losses (power semiconductors and magnetics), input and output current ripple cancellation, improved dynamic response and better modularity, among others. The IBC converter as BDR has been previously treated and advantages and drawbacks discussed. In this paper a new approach is proposed, a multi-switch, multi-phase interleaved boost converter (named Multi Interleaved Boost Converter, MIBC) that provides inductor and switching frequency decoupling, which in turn affects in different aspects, such as, magnetics, input and output current ripples or part count. This paper presents and describes the MIBC, the potential benefits compared to the IBC and its application as BDR.

1. INTRODUCTION

This paper is meant to be a general description of a PWM interleaved method for DC/DC converters. This modulation scheme is aimed to increase converter power density by combining number of modules (phases) in parallel and number of switches per module, please refer to figure 1.

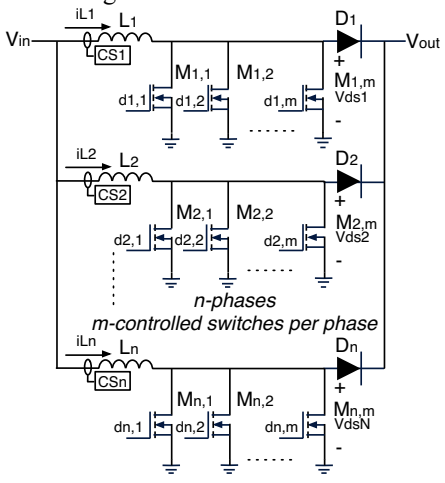

Figure 1. Multi Interleaved Boost Converter

2. MIBC DESCRIPTION

The MIBC has been devised using several multi-switch boost modules, which are out in phase [1]. Traditional multi-switch approach considers the same driving signal for all switches in order to divide the current into several power semiconductors being the reasons for that insufficient current handling capability, excessive power dissipation, complex thermal management or switch redundancy. In the MIBC, the driving signal of each power switch keeps the same switching frequency but the on-time is reduced by a factor *m* and they are displaced each other in phase over *2pi/m* radians. This driving scheme decouples switching frequency and inductor frequency, which actually increases by a factor *m*. Also the common point, mosfet drain, has an effective switching frequency *m* times higher than switching frequency. Another interesting feature is that only one switch conducts at a given time, so average current sharing could be adjusted by increasing the number of switches and decreasing the on time.

On the other hand, phase shifted paralleled modules, so-called interleaved converters, also offer reduction of input and output current ripple, improved dynamic response or power losses distribution, among other advantages. For the MIBC, modules will be displaced *2pi/(nm)* radians.

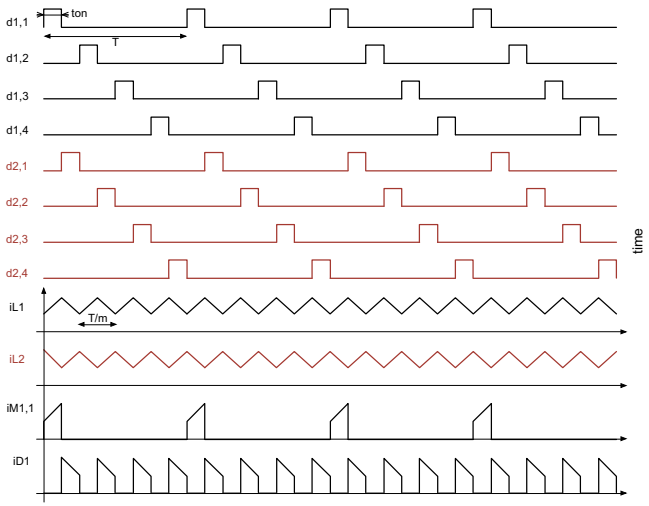

Figure 2. Sketch of the main waveforms of a 2-4-MIBC (2 phase, 4 switches per phase)

2.1 DC equations

The MIBC DC analysis has been performed for the general (n x m) configuration. Main equations are listed in table 1.

Descrip.	Equation	nb
Duty cycle	$D = \frac{t_{on}}{T}$	1
Voltage conversion ratio	$M = \frac{V_o}{V_{in}} = \frac{1}{1-mD}$	2
Inverse voltage conversion ratio	$M' = 1/M$	3
Inductor current ripple (pk-pk)	$\Delta i_L = \frac{1}{m}\frac{V_o M'(1-M')}{Lf}$	4
Average inductor current	$\langle i_L \rangle = \langle i_{in} \rangle / n$	5
Max. inductor current	$i_{L\max} = \langle i_L \rangle + (\Delta i_L/2)$	6
Min. inductor current	$i_{L\min} = \langle i_L \rangle - (\Delta i_L/2)$	7
RMS inductor current	$I_{RMS\ L} = \sqrt{\langle i_L \rangle^2 + (\Delta i_L^2/12)}$	8
Inductor frequency	$f_L = mf$	9
Minimum input current for CCM	$\left\langle i_{in\min_{CCM}} \right\rangle = n\frac{V_{in}D}{2Lf}$	10
MOSFET average current	$\langle i_M \rangle = D\langle i_L \rangle$	11
MOSFET RMS current	$I_{RMS\ M} = \sqrt{D} I_{RMS\ L}$	12
Diode average current	$\langle i_D \rangle = (1-mD)\langle i_L \rangle$	13
Diode RMS current	$I_{RMS\ D} = \sqrt{1-mD} I_{RMS\ L}$	14
Ripple cancellation index	$R = M' \mod n^{-1}$	15
Input current ripple (pk-pk)	$\Delta i_{in} = \frac{n}{m}\frac{V_o}{Lf} R\left[\frac{1}{n} - R\right]$	16
Input (output) frequency	$f_{in(out)} = nmf$	17
Output RMS current	$I_{\underset{\text{RMS}}{out}} = \langle i_{in} \rangle \sqrt{\frac{\left[\left(D'_e - \frac{X}{n}\right)\left(\frac{X+1}{n} - D'_e\right)\right] + \frac{n}{12D'_e}\left(\frac{V_{in}D}{L\langle i_{in}\rangle f}\right)^2}{\left[(X+1)^2\left(D'_e - \frac{X}{n}\right)^3 + X^2\left(\frac{X+1}{n} - D'_e\right)^3\right]}}$ $D'_e = 1 - mD \ ; \quad X = \text{floor}(nD'_e)$	18

Table 1. DC equations of the general (n x m) MIBC converter

2.2 Small-signal transfer functions

Neglecting all parasitic elements, the small-signal transfer functions of the general (n x m) MIBC converter have also been obtained and listed in table 2.

Descrip.	Equation	nb
duty cycle-to-output voltage	$G_{vd} = \frac{\tilde{v}_o}{\tilde{d}} = K_{vo/d}\frac{(1-s/\omega_z)}{(s/\omega_o)^2 + s/Q\omega_o + 1}$ $K_{vo/d} = mV_{in}/D'^2_e; \ \omega_z \simeq nD'_e R/L;$ $\omega_o = D'_e/\sqrt{(L/n)C}; \ Q = D'_e R\sqrt{(nC)/L}$	19
Duty cycle-to-inductor current	$G_{id} = \frac{\tilde{i}_L}{\tilde{d}} = K_{iL/d}\frac{(s/\omega_{z1}+1)}{(s/\omega_o)^2 + s/Q\omega_o + 1}$ $K_{iL/d} = 2m\langle i_{in}\rangle / nD'_e; \ \omega_{z1} = 2/RC$	20
Inductor current-to-output voltage	$G_{vi} = \frac{\tilde{v}_o}{\tilde{i}_L} = \frac{\tilde{v}_o}{\tilde{d}}\left(\frac{\tilde{i}_L}{\tilde{d}}\right)^{-1} = \frac{K_{vo/d}}{K_{iL/d}}\frac{(1-s/\omega_z)}{(s/\omega_{z1}+1)}$	21

Table 2. Small-signal equations of the general (n x m) MIBC converter

3. COMPARATIVE STUDY: 8-IBC vs 4-2-MIBC vs 2-4-MIBC

In order to evaluate and compare the MIBC and the IBC converters used as BDRs, a theoretical study has been carried out using [2] as the baseline specifications, please refer to table 3.

Comparative study: BDR main parameters	
Po	1.6kW
Vin min	56V (mD)max=0.44
Vin max	94V (mD)min=0.06
Vo	100V
L	50uH
Co	88uF
fs	125kHz

Table 3. BDR power module specifications for converter comparison

The study assumes the following, three configurations are evaluated: a) n=8, m=1; b) n=4, m=2; c) n=2, m=4. All have the same number of MOSFETs and consider the same parameters, listed in table 3.

3.1 Input & output current ripple

Substituting values in the equations (16) and (17) result in the input and output current ripples represented in figures 3 and 4.

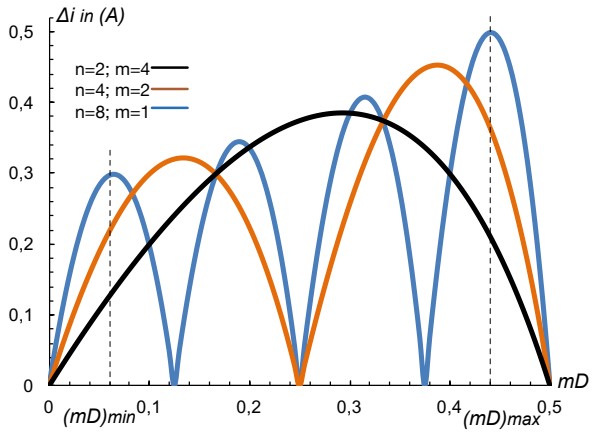

Figure 3. Input current ripple

As observed from figure 3, the 2-4-MIBC configuration exhibits the lowest input current ripple of all three. For certains *mD*, 4-2-MIBC and 8-IBC configurations have less input ripple, but at the extreme values of the duty cycle 2-4-MIBC performs better.

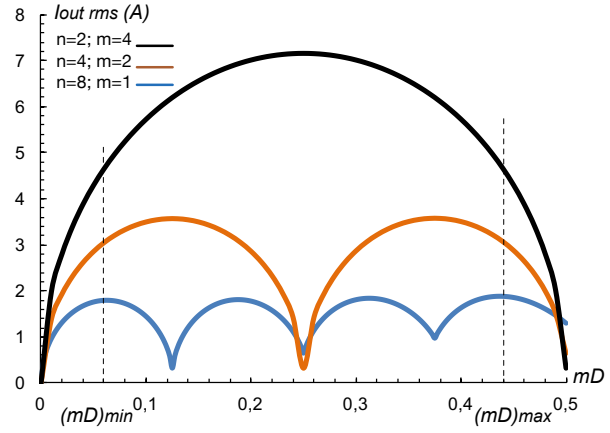

Figure 4. RMS output current (@Vin=56V, Po=1.6kW)

From the point of view of the output current, the 2-4-MIBC has the highest RMS value in the whole range, which is a key parameter for output capacitor losses and voltage ripple. Thus, low ESR capacitors are mandatory to not impair MIBC performance.

3.2 Inductor design

Inductor design, using Magnetics toroid MPP cores, has been considered to evaluate size and volume reduction using MIBC. The inductor design considers Dmax and Po max, the same inductance value and switching frequency for all three configurations. The design procedure has been tuned to achieve similar inductor losses (global losses considering the sum of all inductors) and temperature increment. The most representative inductor parameters have been gathered in table 4.

Comparative study: inductor design			
	n=2; m=4	n=4; m=2	n=8; m=1
Nb of ind.	2	4	8
Iavg	14.2850 A	7.1425 A	3.5713 A
Δi	0.986 A	1.97 A	3.94 A
f	500 kHz	250 kHz	125 kHz
Core ref.	55254	55929	55351
Turns	22	21	34
L[a]	0.051 mH	0.051 mH	0.051 mH
Ploss [b]	8.15 W	4.31 W	2.83W
ΔT	60.6ºC	62.1ºC	56.2ºC
AWG	12	15	18
Win. fact.	18.3%	24.8%	21.5%
DC res.	6.51 mΩ	9.58 mΩ	24.51 mΩ
Finish.OD[c]	45.5 mm	31.1 mm	26.8 mm
Finish.HT[d]	20.1 mm	15.4 mm	12.1 mm
Area [e]	20.70 cm^2	9.67 cm^2	7.18 cm^2
Mass	128.8 g	50.5 g	27.6 g
Total loss.	16.3 W	17.24 W	22.64W
Total area	41.4 cm^2	38.7 cm^2	57.4 cm^2
Total mass	257.6 g	202 g	220.8 g
a) L at full load; b) Ploss per inductor; c) Finished Output Diameter; d) Finished Height; e) Area as OD^2			

Table 4. Inductor comparison

From table 4, 4-2-MIBC exhibits the best outputs in terms of total area and mass, 2-4-MIBC has the lowest losses and 8-IBC gives the poorest results in terms of losses and required size, bringing to light that MIBC offers less input ripple, less losses and less area and mass if compared to the traditional IBC.

3.3 CCM/DCM boundary

Another interesting feature concerns to CCM and DCM limits when MIBC is considered. As the number of phases and inductor frequency changes, the minimum inductor current also varies. Since boost transfer functions depend on conduction mode, the wider the range in a particular mode, the better from the control point of view. Analysing the three configurations, please refer to table 5, one realises that 2-4-MIBC requires the lowest output power to remain in CCM.

Comparative study: CCM/DCM boundary			
	n=2; m=4	n=4; m=2	n=8; m=1
Iin min avg CCM	0.986A	3.94 A	15.8 A
Pin min CCM	55 W	221 W	883 W

Table 5. CCM/DCM limit comparison

Table 5 reveals that 8-IBC requires more than 880W to work in CCM. In other words, 8-IBC will work in both, DCM and CCM, in real conditions. On the contrary, 2-4-MIBC only requires 55.2W to work in CCM; thus, problems related to DCM operation, like parasitic ringing or control loop design are virtually eliminated.

3.4 Power semiconductor stress and impact on losses

An important concern regards to part electrical rating, subsequent part selection and converter losses. One of the most significant differences between the three configurations relates to conduction time and maximum current per switch. Regarding the power mosfet, reduction of both, phases and conduction time per mosfet, implies identical average current value, similar RMS value but higher peak current. Two important considerations arise from this fact, higher peak current capacity will be required and switching losses could increment substantially. Since all configurations will exhibit similar conduction losses, soft-switching techniques can be explored to keep similar performance. Regarding power diodes, one diode per phase is only required, but working at higher current level and *m* times switching frequency. Parallel diodes could be also considered to split power losses.

Comparative study: electrical rating (Vin=56V, Vo=100V, Pin=1600W)			
	n=2; m=4	n=4; m=2	n=8; m=1
Conduction time	0.88us	1.76us	3.52us
MOS avg current	1.57A	1.57A	1.57A
MOS RMS current	4.74A	3.35A	2.34A
MOS max. current	14.78A	8.13A	5.54A
D·(Irms mosfet)^2	$2.47A^2$	$2.47A^2$	$2.49A^2$
DIODE avg current	8A	4A	2A

Table 6. MIBC electrical rating

3.5 Small-signal transfer functions

The MIBC small-signal transfer functions depend on both, *n* and *m* parameters. The number of phases, *n*, determines the equivalent inductance whereas the number of devices, *m*, has impact on the duty cycle.

Figures 5 and 6 represent the Bode plot of the small-signal transfer functions Vo/d and iL/d obtained by the PSIM simulator for the configurations specified in the table 7.

Comparative study: small-signal transfer functions (Vin=56V, Vo=80V, Pin=1024W)			
	n=2; m=4	n=4; m=2	n=8; m=1
Kvo/d	53.2dB	47.2dB	41.2dB
fz	19.5kHz	39kHz	78kHz
fo	2.37kHz	3.36kHz	4.75kHz
Q	8.21	11.6	16.4
Kil/d	40.4dB	28.3dB	16.3dB
fz1	579Hz	579Hz	579Hz

Table 7. MIBC small-signal transfer functions

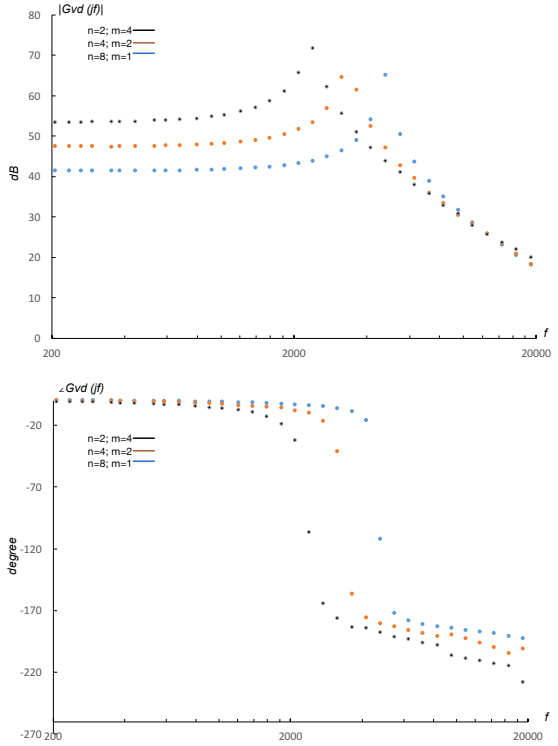

Figure 5. Duty cycle-to-output voltage transfer function. PSIM non-averaged model (Vin=56V, Vo=80V, Po=1024W)

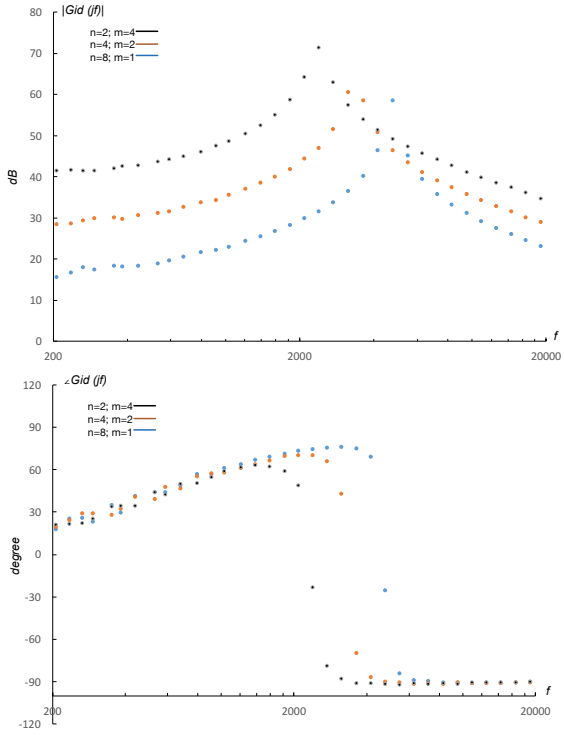

Figure 6. Duty cycle-to-inductor current transfer function. PSIM non-averaged model (Vin=56V, Vo=80V, Po=1024W)

4. MIBC SIMULATION

Computer simulations using PSIM (Powersimtech) have been carried out to compare different configurations: a) n=2; m=4, b) n=4; m=2, c) n=8; m=1, using the values of Table 3.

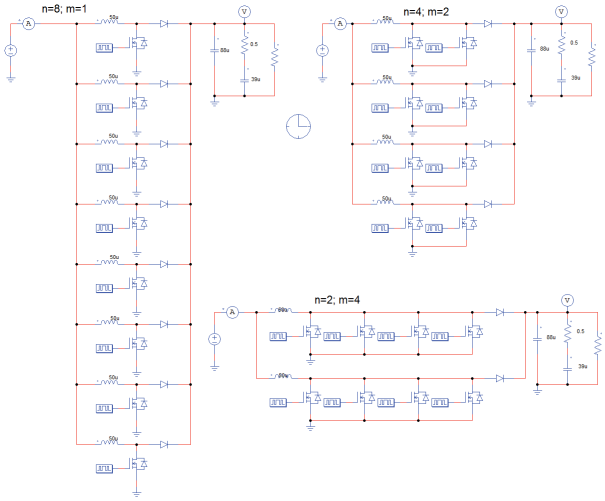

Figure 7. MIBC different simulation schemes.

Input current ripple at the minimum input voltage and maximum power for each configuration is represented in figure 8. The lowest input current ripple corresponds to the n=2; m=4, according to (16) and figure 3.

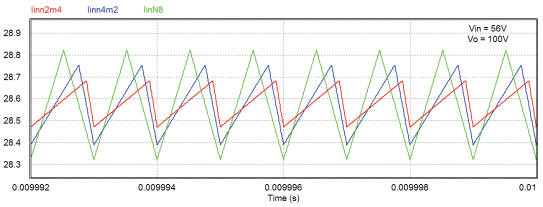

Figure 8. Input current ripple.

Output capacitor current at the minimum input voltage and maximum power for each configuration is represented in figure 9. The lowest RMS value corresponds to the n=8; m=1, according to (18) and figure 4.

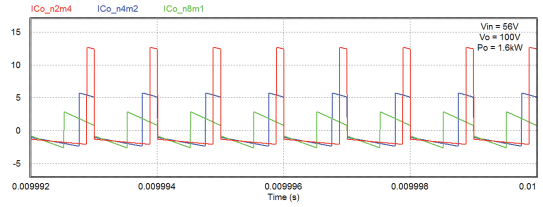

Figure 9. Output capacitor current.

CCM/DCM boundary is represented in figure 10. Considering a load resistor of 181.82 ohms (55W@100Vo), only the n=2; m=4 configuration keeps in CCM operation due to higher inductor frequency. The other two configurations, in open loop mode, increase the output voltage because of DCM operation.

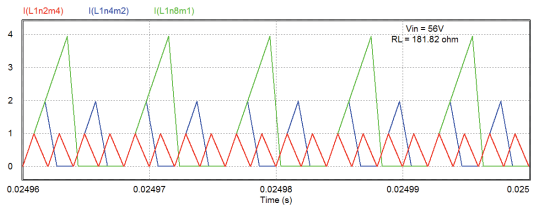

Figure 10. Input current ripple.

Mosfet current is depicted in figure 11. As it can be observed, the average value is the same for all configurations but the peak value and RMS value is higher as *n* decreases.

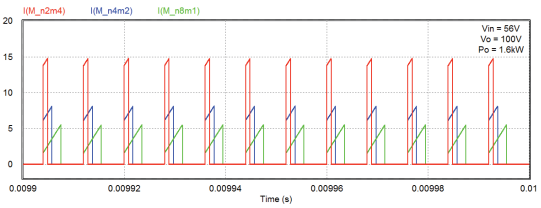

Figure 11. Mosfet current.

5. MIBC: ANALOG PWM GENERATOR

Two methods have been devised to obtain desired PWM signals for the MIBC. First method uses *n* sawtooth signals and the control signal (Vc) splits into *m* signals (Vci) with different offset (Voi), (22).

$$V_{Oi} = (i-1)\frac{V_p}{m} \quad ;i = 1..m \tag{22}$$

$$V_{ci} = V_c + V_{Oi}$$

Simplified block diagram of the PWM generator for the 2-4-MIBC and the sketch of the main signals are depicted in figure 12.

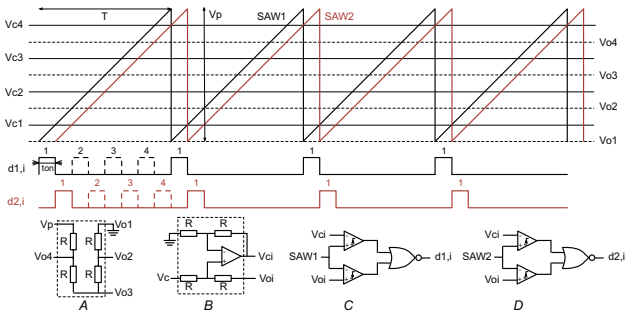

Figure 12. Analog PWM: option 1.

Another option is to use *n·m* sawtooth signals and only one control signal, which is limited to *Vp/m*. Figure 13, shows the sketch of this analog PWM generator. Only one comparator is required for each driving signal.

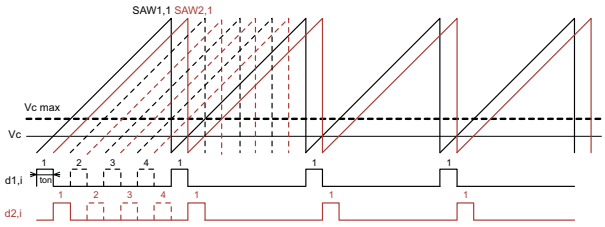

Figure 13. Analog PWM: option 2.

Figure 14 represents the PWM signal (d1,1) and the sawtooth (SAW1,1) of one power MOSFET using the second method with the commercial multiphase integrated oscillator LTC6909 and a constant current source that charges a capacitor.

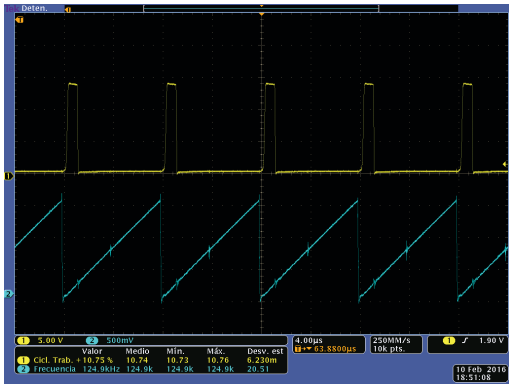

Figure 14. Sawtooth and PWM signal: option 2.

6. MIBC: DIGITAL (FPGA) PWM GENERATOR

Analog implementation of the PWM generator offers simplicity as the main advantage. On the contrary, digital approach, FPGA is considered here, is more complex but has some benefits that should be considered. To highlight some, high time resolution to achieve very low duty cycles, synchronous signals with adjustable dead time for bidirectional conversion or soft-switching, hot reconfiguration for redundancy, protection or efficiency purposes.

In this paper a digital PWM adapted from analog method option 1 is presented. Figure 15 shows the four gate signals of one phase switching at 96kHz.

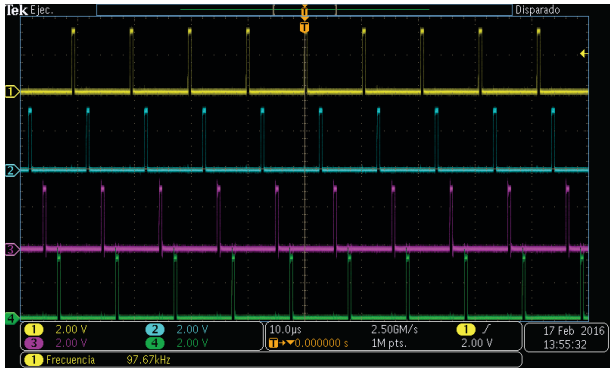

Figure 15. Digital PWM signals for one phase: adapted from circuit option 1.

7. CONCLUSIONS

This paper presents an interleaving technique that is suitable for DC/DC converters, BDR's is one possible application, as studied here, but other power conditioning functions could be explored. Design equations, comparative study and analog and digital (FPGA) practical implementation of the PWM generator system is presented.

8. REFERENCES

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