EFFICIENT POINT OF LOAD CONVERSION FROM THE SATELLITE MAIN BUS

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ABSTRACT

This paper examines some of the issues involved in the distribution of power from the Main Satellite bus to advanced Mixed Signal Electronics payloads. Trade-offs are described in the design of Bulk voltage conversion vs Point of Load conversion. These trade-offs should support mission objectives of high efficiency, fault tolerance and control of crosstalk between subsystems.

1. INTRODUCTION

Satellite digital processing systems present demanding requirements for power distribution from the vehicle's main power bus down to regulated power rails on FPGA devices such as RTG4 FPGAs, Microsemi's fourth-generation flash-based FPGA. Heritage systems consist of bulk sub-bus power converters, typically 5V outputs, driving a number of parallel load assemblies with low impedance distribution and good local decoupling to maintain adequate Point of Load (POL) regulation. The lower voltage rails and higher dI/dt transient requirements of advanced processor systems drive a requirement to integrate bulk power conversion into processor load module printed wiring assemblies (PWAs) for improved regulation and fault tolerance. This paper discusses these regulation issues, broader issues of isolation and fault tolerance and the solutions offered by Microsemi's SB30 bulk POL DC-DC power converter, which in this paper is termed a "Point of Module" converter.

2. FPGA POWER REQUIREMENTS

A generalized concept for PWA power distribution to the FPGA is illustrated in Figure 2.1 [1]

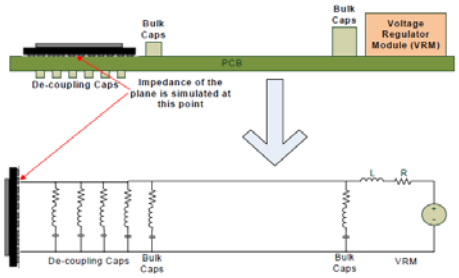

Figure 2.1 FPGA General Power Distribution

Impedance to the power rails must be sufficiently low to maintain static and dynamic voltage regulation limits for the main FPGA functions.

Taking the example of Microsemi's new RTG4 FPGA; power supply requirements are classified as:

- Core (1.2V; 1.5A, up to 8A)
- Input /Output (3.3V; 500mA)
- Serializer/Deserializer (SerDes) (1.2V; 250mA)
- Double data rate (DDR) (1.5V; 250mA)
- Phase-locked Loop (PLL) (3.3V; 10mA)

3. BUS IMPEDANCE CALCULATIONS

Complex FPGA designs have increasing amounts of current transients switching across the power bus. Simultaneously switching outputs (SSO) contribute to a major share of instantaneous current issues. Decoupling with low effective series inductance capacitors provides localized high frequency energy to decouple noise from the switching currents of the device power bus. This is most effective when capacitors are in close proximity to the device. Some of these high frequency capacitors are required to be placed directly by the FPGA.

Target impedance is calculated based on Eq 1:

$$Z_{Min} = \%\ Ripple \times \frac{V_{supply}}{I_{trans}} \quad (1)$$

Vsupply: Supply voltage of the power plane

% Ripple: Percentage of ripple allowed on the power plane

Itrans: Transient current drawn on the power plane. Generally, transient current is half of the maximum current.

Zmin: Target impedance of the plane

4. POINT OF MODULE POWER DISTRIBUTION CONCEPT

4.1. Point of Module Power Distribution Considerations

What is desirable for a Module Level power converter? The following features should be considered:

- Bus facing EMI performance
- Bus isolation
- Fault containment
- Fault isolation
- System efficiency
- Number of Bulk supply rails
- Tradeoff between bulk power conversion and POL power conversion, driven by serviced load regulation requirements

4.2. EMI Performance

For general EMI compatibility MIL-STD 461 establishes emission requirements and complementary susceptibility performance that guarantees compatibility between power converters on a bus distribution system. In heritage sub-bus distribution systems several load modules would connect on a sub-bus with no intermediate filter. In a number of applications, notably communications satellites, it is important to isolate noise between channels. A module level regulator with galvanic isolation and a MIL STD 461 EMI compliant filter provides excellent channel to channel isolation for these applications

4.3. Bus Isolation

The important benefit of using an isolating bus converter to connect the Module to the satellite main bus is the ability to establish ground potential on the load side independent of the Main Power bus common potential. Now the potential of the Module's local ground is insulated from steady state and transient voltage variations that may occur on the Main Bus. Signal interfaces between modules are therefore maintained with optimum signal to noise margins.

4.4. Fault Containment

Satellite systems are often arranged in N+M redundant configurations to provide for graceful degradation and prolonged mission life. The Point of Module converter already provides good fault isolation performance through its galvanic isolation and load current limit function.

4.5. Fault Isolation

Further security from Failure Mode Effects may be provided by a fuse at the converter input that opens in the event of an internal high current fault. A further refinement to this is a Solid State current limiter / resettable fuse that will limit the load current during the fault event and help preserve Main Bus voltage.

4.6. System Efficiency

Larger Satellites with higher power use higher Main Bus voltages to transmit power to the payload systems. 100 volt bus is now common The International Space Station (ISS) has 120V operating up to 165V transient. The ideal for size and weight is a single stage conversion from main bus to user voltage. However with FPGA core voltages running as low as 1 volt with potential still to move south, a 100:1 voltage conversion ratio becomes unwieldy.

4.7. Number of Bulk Power Supply Rails

The number of power converter output rails is determined by the module load configuration. Generally a 5V bulk rail is provided for distribution to downstream POL regulators. 3.3V down to 2.5V bulk rails can also be provided for Input / Output and other "non-core" functions that don't have large load transient requirements and have relatively wider line regulation tolerance.

4.8. Load Power Allocations to Bulk and POL

The specific choice between on module bulk supply rail usage and POL usage must be determined by the Mixed Signal module designer based upon steady state and transient regulation requirements achieved considering on-PWA bus distribution impedances. In a general case an efficient POL converter transforms the source impedance of the bulk bus by the square of its voltage transformation ratio over its effective closed loop control bandwidth. This enables the energy in a local decoupling capacitance to be stored more efficiently at a higher voltage level.

5. SB30 ARCHITECTURE CONCEPT

In traditional power distribution a bulk sub-bus converter supplies power to parallel connected mixed signal processor modules (PWA's).

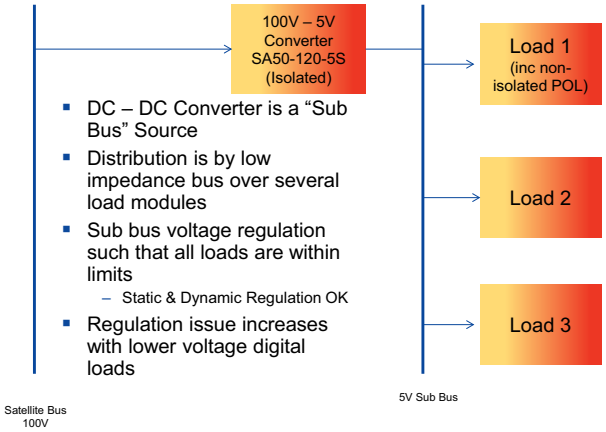

Fig 5.1 Traditional Heritage Sub Bus Power Distribution

As device supply voltages drop and current levels increase the regulation performance of the traditional approach becomes problematic and "Point of Module" power regulation becomes preferable.

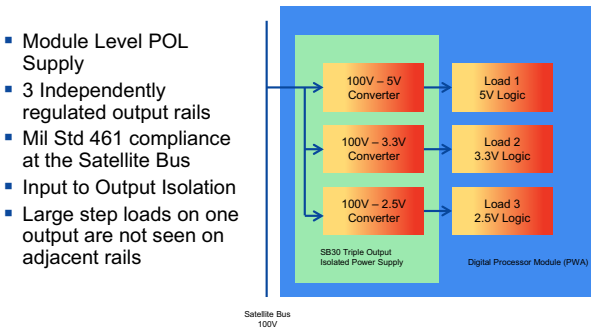

Fig 5.2 Main Bus Distribution to Point of Module Concept

In the Point of Module concept, main satellite bus power is brought to the Payload module input and an on board power converter directly generates necessary bulk voltages for internal distribution on the module.

The SB30 DC-DC Converter and its optional associated Self-Resettable Fuse (SRF) connect directly to the satellite main bus and provide the following services:-

- Efficient, direct conversion from the Main Bus to on- module power distribution rails
- 3 Independently Adjustable Regulated Outputs,
- Power Rail voltages are programmable between 5V and 2.5V.
- Embedded EMI filtering with a high rejection of noise coupling to other systems
- Flexible bus input voltage, 28V to 100V
- Hiccup overcurrent protection
- Fault disconnection from the Satellite power bus
- Enhanced PWA distribution impedance model, transient and static

The SB30 Power Conversion topology is shown in Figure 2. [2]

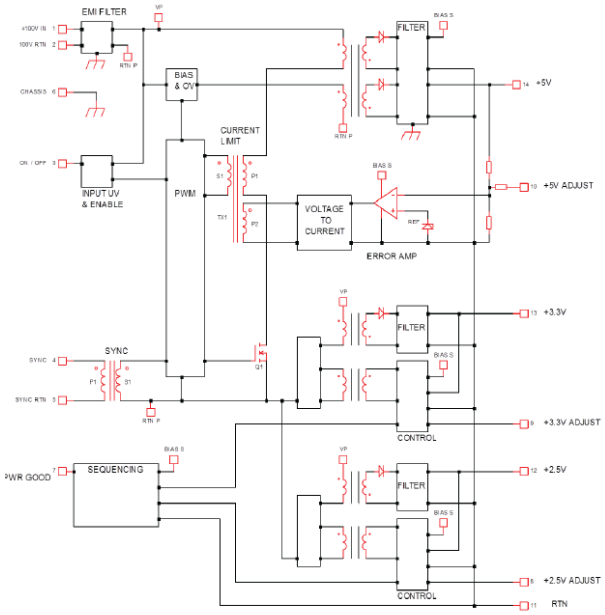

Figure 2: SB30 Power Conversion Topology

The primary power conversion channel converts the 100V Main Bus input to 5V bulk output using a primary side PWM controlled flyback converter. Output voltage is sensed and compared with a secondary side reference to produce an output voltage error signal. This signal is converted to a proportionally pulsed current signal that is combined with sensed primary current to deliver pulse by pulse feedback to the PWM controller. This "V + I" feedback control delivers excellent static and dynamic output voltage regulation performance.

The 5V output channel then powers the secondary side controllers for the other 2 power conversion channels. These auxiliary power converters are also flyback converters. This topology produces 3 independently regulated output rails all with independent current limit protection. Each channel has single stage conversion from the main bus to each output rail.

6. FAULT ISOLATION THROUGH ACTIVE POWER DISCONNECT

The main bus input to the Point of Module power

converter can be provided with additional protection against downstream load faults through the series connection of a Self-Resettable Electronic fuse. This concept which is currently in product development provides a soft turn on switch into the power converter and limits then turns off the current according to a preset I^2t overload profile. The device is configured to retry the load at pre-determined intervals to check for fault clearance and can be permanently turned off if this does not occur.

The concept for this electronic fuse is shown below:

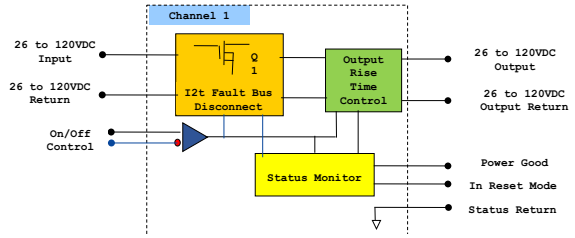

Fig 6.1 Electronic Fuse Concept

In applications that require it, the Electronic fuse can parallel connect 2 redundant power sources into the Point of Module power converter.

7. THE FULL SOLUTION

The concept for the full Point of Module Power Distribution system is shown below:

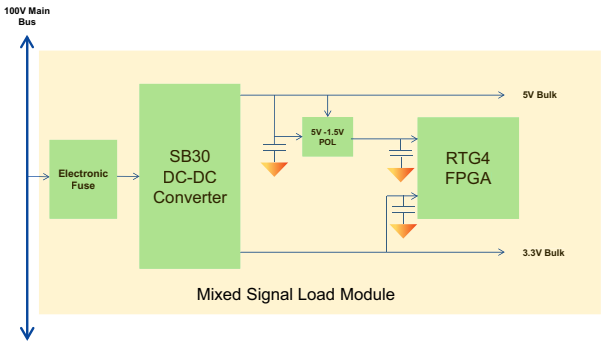

Fig 7.1 Full Point of Module Distribution Concept

Note the local decoupling capacitors at the FPGA which decouple the fast logic transition edges and the local decoupling capacitor at the POL converter which limits the transient voltage from a step load change in the FPGA Core power demand.

8. CONCLUSION

The SB30 Point of Module design concept combined with electronic fusing enables an optimal power conversion and distribution scheme for modern space digital FPGA and processor systems where conversion efficiency, fault tolerance and well regulated power rails are of paramount importance for robust and reliable solutions.

9. REFERENCES

1. Microsemi application note AC453; Layout Guidelines for RTG4-Based Board Design
2. Microsemi Datasheet: SB30-100 Triple Series; Radiation Hardened Isolated DC/DC Converters