A NEW, SINGLE DIODE, SEQUENTIAL SWITCHING SHUNT REGULATOR

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ABSTRACT

This paper describes the design improvement of a Sequential Shunt Switching Regulator (S3R) based on a power cell composed of one switching FET and one Diode connecting the Solar Array (SA) section to the Main Bus.
This topology allows to minimize the S3R cells dimensions, to optimize the efficiency figures and complies with the electrical Single Point Failure Free (SPFF) requirement on the Main Bus.
The single switching FET can cause the loss of one Solar array section if it fails in short circuit, while its failure in open can be compensated by the presence of one additional (spare) shunt section positioned on Main Bus to drain the power eventually in excess.
If the series redundancy of the Diode is removed, its failure in short circuit, causes overload on the Main Bus when the switching FET turns ON. To avoid the possible subsequent failure in short circuit of the switching FET due to over-heating, with permanent loss of Main Bus, the maximum current drawn by the FET in failure condition and the duration of this operation mode must be strictly controlled in order to avoid thermal overstress and consequently thermal failure propagation.
The adopted solution foresees a circuitry that controls the current in the FET, both the peak in the first transient and the subsequent limited value, and forces the FET in permanent open status after a short period, compatible with the overheat of the FET junction.
No spurious cause leads to the permanent loss of the S3R section due to permanent activation of the protection, causing the switching element (FET) to be continuously open.
In fact a dedicated circuit, activated by sensing of the Error Signal, unlatches the section to restore the power control.
The presented design has found its first application in the PCDU for the COSMO-SkyMed Second Generation (CSG) satellite power system.
A dedicated Elegant Bread Board of the S3R, integrated with the board designed to control the Battery Current and Voltage has been tested in the design and development plan of CSG PCDU.

1. S3R DEVELOPMENT AND SYSTEM OVERVIEW

The Sequential Shunt Switching Regulator (S3R) has been developed to control the power delivered from a Solar Array (SA) made of 16 sections to condition an unregulated Bus where the Battery Charge Current and Voltage are regulated.
The application has been developed to control a SA and a Battery with the following characteristics:

- 10 Li_ion battery modules each up to 24Ah.
- Battery Voltage from 41V to 68V.
- 16 Solar Array sections.
- Isc = 5A max.
- Voc = 140V max.
- SAS capacitance = 1uF max.

The S3R solution was adopted for its simplicity and cheapness, also because it was not required the MPPT control.
Furthermore, the need for a reduction in space occupation of the S3R cells as well as of their dissipation due to the stringent space available in the Power Conditioning and Distribution Unit (PCDU) in the frame of the COSMO Second Generation program, suggested the single Diode S3R solution.

2. S3R OPERATION

Each S3R cell can operate in three different ways:

- Conduction mode: the cell delivers all power from the SA section to the battery bus;
- Shunt mode: the cell absorbs all the current from the SA section;
- Switching mode: the cell switches between conduction and shunt modes, thus modulating the power delivered to the bus.

Depending on the power demand, in order to control the charge parameters of the Battery (voltage and charge current), the system determines via an Error Signal, the number of S3R cells in conduction and in shunt mode and which S3R section is regulating (switching) its current.
The system is designed so that only one cell at once may operate in switching mode.

3. S3R FUNCTIONALITY AND FAILURE PROTECTION

Fig. 1 depicts the block diagram of the S3R Cell.
Details of the blocks are given in the following paragraphs.
The shunt MOSFET is turned on whenever the current

from that SA section is not required by the Bus loads. This case occurs when the total power that the SA can deliver exceeds the demand of the system and the control logic responds by 'shunting' one or more sections.
On the contrary when the current from the SA section needs to be delivered to the bus, the MOSFET is turned off, allowing the diode to conduct.

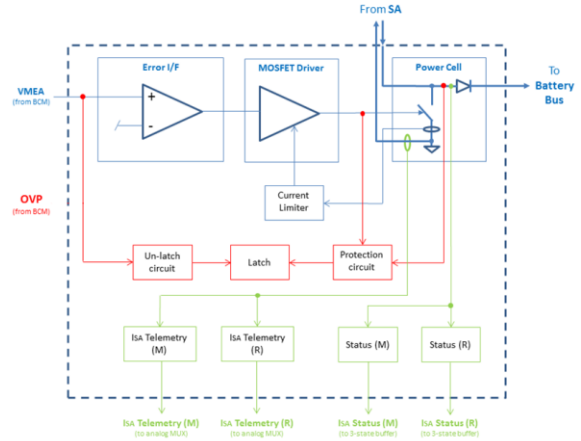

Figure 1. S3R Cell block diagram.

The topology of the power cell is visible in Fig. 2. It guarantees the shunt regulation with minimal component count, thus allowing space and cost saving.
Besides an efficiency above 98% has been estimated for power transfer to Main Bus, with bus voltage above 50V and section current up to 5A.

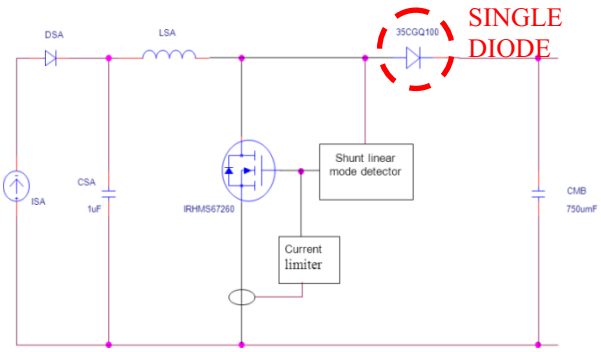

Figure 2. One-series-diode S3R Cell Configuration.

One failure inside PCDU can cause, as worst condition:

- Short circuit of the shunting element (FET). It causes the short circuit to ground of one Solar Array section only, without propagation to other 15 sections and to the system.
- Short circuit of the series diode. It causes one Solar Array section to be permanently connected to the BATT_PWR_Bus. In case of intervention of the shunt FET this condition is very dangerous for the system causing a permanent short circuit on Main Bus.

Normally the series redundancy is applied to control this second failure mode.
The improvement of the presented design is based on the electronic control of such a condition using the shunting element of the power cell to sustain and remove the dangerous operation.
To get this aim a Latching Current Limiter, positioned on the switching leg of the S3R section will trip and force the shunting FET to be permanently opened (latched), to prevent Main Bus overload, in the case the shunt element is commanded closed in presence of the short circuit of the diode.

4. S3R CURRENT LIMITATION

Current Limitation is necessary to prevent overload on Main Bus. Besides the current limiter must force and latch the shunt MOSFET in open.
The definition of the limitation value is limited downwards to optimise the power losses during switching in normal operation, and upwards to guarantee the survival of the FET itself to the failure event.
Due to the criticality of the application the limitation design, to guarantee the reliability of the MOSFET after the intervention of the protection, must guarantee that:

- The maximum peak current do not exceed, by design, the maximum acceptable value specified (180A is the rated one for the device used), derated at 75% (as per ECSS-Q-ST-30-11C-Rev1 relevant to the maximum I_{DRAIN}).
- The maximum temperature of the junction of the switching device (FET) must remain below 110°C, according to ECSS-Q-ST-30-11C-Rev1, during the whole limitation period. The junction temperature rise is caused by two main contributions, during the limitation phase before the trip-off intervention:
  - Initial (peak) transient.
  - Actual Limitation period.

It must be noted that the entity of the maximum peak current is relevant as regards both the MOSFET junction temperature rise and the current capability of the bonding inside the device (fuse effect for too-high currents). The former aspect has been evaluated in the dedicated computations regarding the MOSFET junction temperature rise. The latter has been clarified by the MOSFET manufacturer that provided the plot with the "Fuse Current" of the bonding as function of the overcurrent duration. The plot is reported in Fig. 3.
With the peak current duration observed both in para. §5 and §5.2, in the order of 300nsec, a very high current can be sustained by bonding without any risk.
So, the chosen approach to use the maximum derated value as acceptable value for the peak current of the MOSFET is a very conservative approach.

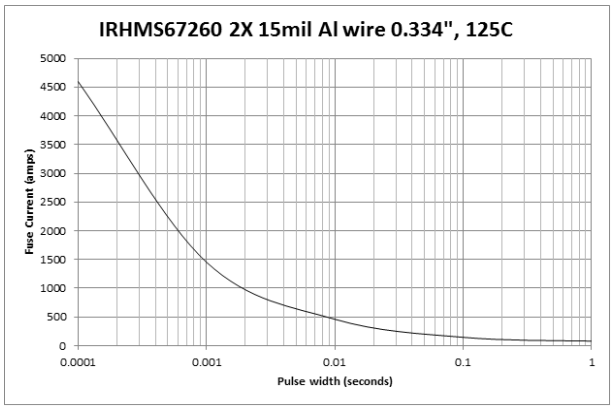

Figure 3. Sensitivity of MOSFET bonding to Pulsed Over Current.

The protection is designed to be active also in case of unit powering in presence of a (latent) failure of one diode in short circuit.

The definition of the limitation value moves from the control of the switching losses and of the current peak during turn-on and turn-off transients.
The switching losses are mainly related to turn-on transient, when the SA capacitance C_{SA} is discharged. In order to avoid large spikes (which can lead to EMC problems or possibly to reliability issues), the discharge current must be limited to a value I_lim (higher than the S/A maximum current I_SA), resulting in higher turn on time. It can be demonstrated that the maximum value of the switching losses is:

$$P_{sw,\max} = \frac{1}{2} C_{SA} V_{bus,\max}^2 \frac{I_{\lim}}{I_{\lim} - I_{SA}} f_{sw,\max} \quad (1)$$

where $V_{BUS,max}$ and $f_{sw,max}$ are the maximum values of the bus voltage and the switching frequency. The equation shows that the higher I_{lim}, the lower $P_{sw,max}$.
As I_{lim} cannot be arbitrarily high an appropriate compromise between peak current and switching losses must be identified.
Fig. 4 shows the normalized power losses in the shunt MOSFET as a function of the ratio I_{lim}/I_{SA}. The power is normalized to

$$P_{\infty} = \frac{1}{2} C_{SA} V_{bus,\max}^2 \frac{I_{\lim}}{I_{SA}} f_{sw,\max}, \quad (2)$$

which is the asymptotic value for $I_{lim} \rightarrow \infty$.

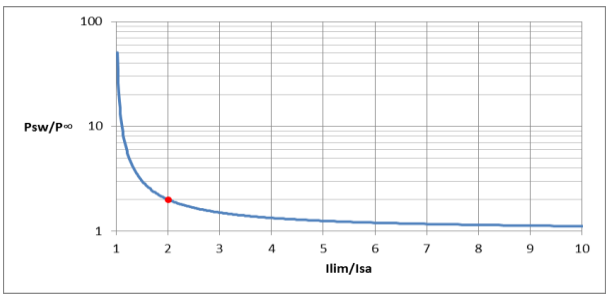

Figure 4. MOSFET switching losses (normalized) as a function of the ratio Ilim/Isa.

Moving from this considerations, a good trade-off in the definition of I_{lim} can be found with a value of I_{lim} equal to about 2 * I_{SAmax}, as further increases in the value of I_{lim} lead to small variations of P_{sw}.
Fig. 5 shows the schematic of the current limitation circuit, where it is shown that an active current limiter and a passive current limiter concur to the function.

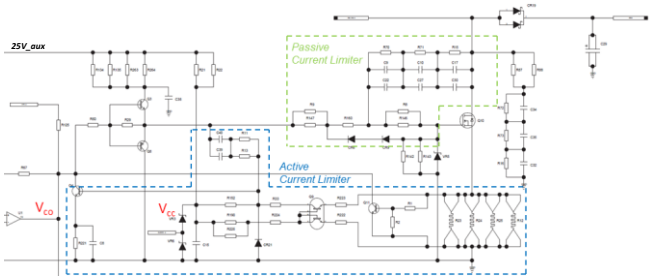

Figure 5. Current Limiter schematic.

4.1. Active Current Limiter

The active current limiter is based on a current mirror sensing circuit surely active during diode short and possibly during normal turn-on transients.
The limitation value is defined by the equation (3), where R_s is the parallel of the four sensing resistors R_{12}, R_{23}, R_{24}, R_{25}, R_c=R_{224}+R_{190}//R_{225}, V_{cc} is the local supply voltage.

$$I_{\lim} = \frac{R_{222} - R_{223}}{R_s} \frac{V_{cc} - V_{be9}}{R_{222} + R_c} \quad (3)$$

The circuit has been dimensioned to obtain I_{lim} = 12A.
As the current limiter has an intrinsic delay in intervention during which the FET current can rise uncontrolled, up to very high values that can easily exceed the rated maximum current, a further "fast acting" current limiter, that opens the Gate-Source of the FET, is implemented (Q_{11}) to speed up the circuit and to control the value of the current peak in case of short circuit of the series diode. This additional limiter is silent in normal operation, as its threshold is defined by:

$$I_{lim,facl} = \frac{V_{be11}}{R_s}, \quad (4)$$

Which is significantly greater than I_{lim}, in the order of 30A.

4.2. Passive Current Limiter

The passive current limiter works (in conjunction with the active circuit) to limit current peaks during turn-on transients.
It limits the discharge rate of the parasitic SA capacitance C_{SA}, by controlling the MOSFET Gate to Drain capacitance charge.
The resulting effect is beneficial for all the turn on

transients, during normal operation or after a diode short circuit event, but it doesn't work if the diode short circuit occurs while the mosfet is shunting, which is the heaviest failure condition.

4.3. Fault Detector and trip-off circuit

Fig. 6 shows the fault detection circuit and LCL trip-off timer.

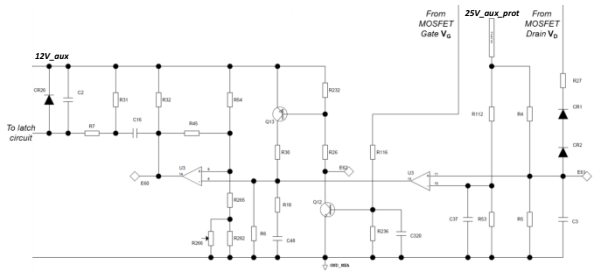

Figure 6. Fault detection circuit.

When a fault is present and the current limiter is activated both the shunt MOSFET gate and drain voltages rise (Gate initially to 12V and successively to V_{gs_th}, during limitation, while Drain to Main Bus voltage).
This condition triggers the fault detection circuit. After a fixed period, defined by the charge of a capacitor (C_{48}) up to meeting a threshold that activates a comparator (U_3), the protection chain acts on the reset of a Flip Flop which latches the status and switches the MOSFET to open.
Of course the protection must not to be triggered during normal operation.
When the S3R MOSFET is off its gate voltage is low and the fault detection circuit is not triggered, so that C_{48} cannot be charged.
When the S3R MOSFET is ON its drain voltage is low and C_{48} charge is inhibited by the port of U_3 activated by the conduction of CR_1 and CR_2.
During the turns on transient of the S3R MOSFET the fault condition is triggered but rapidly removed at the MOSFET closure.
In this case the partial charge of C48 must be sufficiently low to avoid latch-off of the module with adequate margin.
To meet this aim the condition (5) must be satisfied.

$$t_{trip\text{-}off} > t_{turn\text{-}on} \tag{5}$$

Equation (5) sets a lower limit to the Trip-off time.
The maximum value for $t_{turn\text{-}on}$, assuming V_{bus} = 70V, I_{lim_min} = 10A, C_{SA} = 1µF is computed in equation (6).

$$t_{turn-on} = \frac{C_{SA} \times V_{bus}}{I_{\lim} - I_{SA}} = \frac{1\mu\mu \times 70V}{10A - 5A} = 14\mu s \tag{6}$$

On the other side, the upper limit for the trip-off time is set by thermal considerations on the S3R MOSFET when working as limiting element.
Assuming a maximum limitation current of 14A and a maximum drain voltage of 70V, the shunt MOSFET is claimed to dissipate 14A * 70V = 980W.
Considering a mounting temperature for the MOSFET of 70°C the resulting maximum allowable $Z_{\Theta j\text{-}c}$ is

$$Z_{\Theta j-c} = \frac{110 - 70}{980} = 0.41°C/W, \tag{7}$$

which corresponds to a pulse width of about 170µs (from datasheet curves for $Z_{\Theta j\text{-}c}$).
Equations (5) and (6) show that the trip-off time can be set to a value between 14µs and 170µs.
The nominal trip-off time has been set to 100µs.

5. DESIGN VERIFICATION

The behaviour of both the current limitation and the fault protection intervention have been validated both via simulation and by test. The tests have been performed on an EBB representative of the electrical circuit and of the PCB layout.

5.1. Simulation Results

Computer aided simulations with PSpice , using the actual component models, have been performed.
The failure simulation of the series diode of the S3R section has been evaluated in both the following conditions:

1. Short circuit present at MOSFET turn on.
2. Short circuit applied when MOSFET is already on. This condition is heavier than the previous both for the peak current and for the thermal stress of the MOSFET, as the intervention of the switch-on circuit, including the passive limitation, is by-passed, being the MOSFET already on.

The simulations have been performed at 70V Bus Voltage and 5A SA Current, that round in excess the maximum values defined for the reference CSG program.
Fig. 7 shows the simulation result for condition 1.

Figure 7. MOSFET turn on with diode in short circuit.

In the upper box the MOSFET V_{GS} (red trace), together with internal voltages related to the timer are shown, precisely the latch output (green trace) and the voltage of the inverting input of the comparator (U3, pin8)

implementing the protection (yellow trace). The lower box shows the MOSFET I_{DRAIN}.
The limitation transient can be observed, lasting 100µs and limiting current at 12A for a (trip-off). The current peak is very contained (less than 30A). This value is well acceptable as it causes reduced stresses on the limiting device.
Fig. 8 shows the simulation result for condition 2. The V_{GS} (orange trace) and V_{DS} (blue trace) of the MOSFET, together with the latch output (green trace) and the voltage of the inverting input of the comparator (U3, pin8) implementing the protection (red trace) are visible in the window above, while I_{DRAIN} is visible in window below.

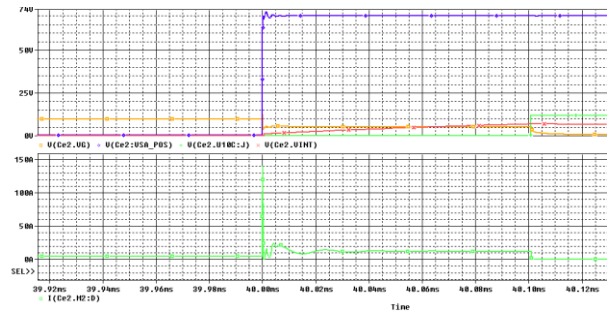

Figure 8. Limitation circuit simulation. Worst case.

The limitation transients is shown in Fig. 8. The limitation Current (12A) and its duration (100µs) are the same as in Fig. 7.
Fig.9***Figure 9*** shows the action of the fast limitation circuit that keeps the current peak below 130A as maximum value. Its shape is triangular, about 250ns in duration at half value.

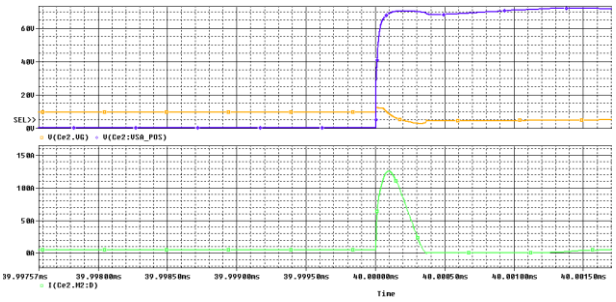

Figure 9. Limitation circuit simulation. Peak control.

5.2. Test Results

The design and the simulation results have been verified on an Elegant Bread Board (EBB) representative of the final design both electrically and for the layout, but not mechanically.
Two S3R boards have been manufactured, tested and integrated with the Battery Control electronics Module (BCM) and with a capacitor bank to reproduce the whole battery charge control function as designed in the frame of the CSG program.
Current Limitation after the short circuit of the series diode has been tested in the same conditions applied in the simulations:

1. Short circuit present at MOSFET turn on.
2. Short circuit applied when MOSFET is already on.

For both the test conditions the failure in short circuit of the series diode has been applied placing across it a Short Circuit Generator.
The current flowing into the FET has been measured in the leg sense resistor (nominal value 15.5mΩ) where the limitation is electronically sensed.

Test condition #1 has been performed on all the S3R sections and at various Bus voltage values, in order to characterise the limitation function. The analysis of the results shows a very contained spread in values and waveforms among the various circuits.
Fig. 10 shows V_{MB} (high end value), MOSFET V_{GS} and I_{DRAIN} current.

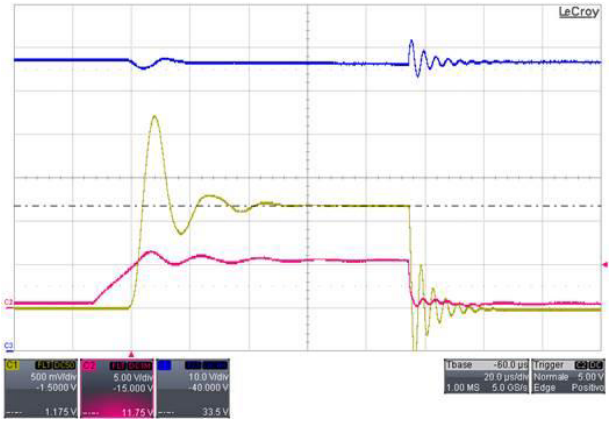

Figure 10. Limitation measurement at Mosfet turn- on.

Test condition #2 has been characterised at both low and high ends of the Bus voltage range, when the FET was conducting, as made for the simulation. This represents the most stressing operating condition for the MOSFET.
The waveforms showing the intervention of the protection are visible in Fig. 11 and in Fig. 12, where the traces have the following meaning:

TR1: Voltage across Rsense. (MOSFET Current).
TR2: V_{DS} of the FET.
TR3: V_{GS} of the FET.
TR4: Internal latch signal.

The maximum measured current peak is about 85A, well inside the simulation results and the acceptability level stated in para. §4.

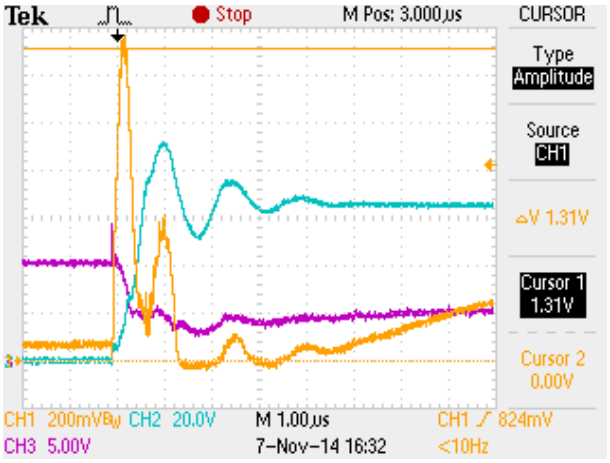

Figure 11. Limitation measurement. Peak control.

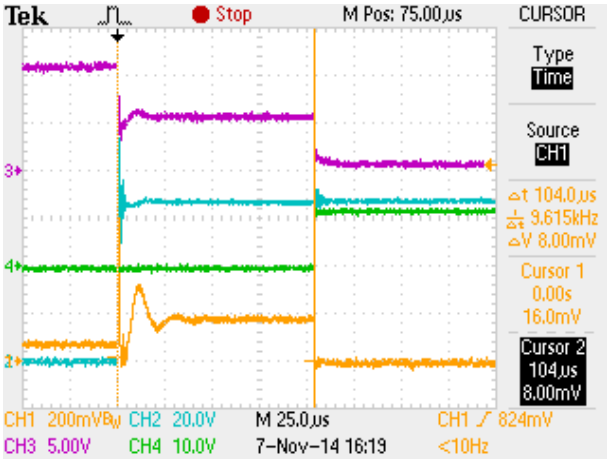

Figure 12. Limitation measurement.

To evaluate the benefit of the adopted solution, dissipation has been also measured during the tests of the full S3R integrated function.
The efficiency of the S3R section has been measured well above 98% at maximum SA power on a temperature range -25°C ÷ +60°C.

5.3. MOSFET Junction Temperature

From the results shown in the paragraph §5.2, the maximum expected temperature rise in the switching elements (FET) can be computed.
Moving from waveforms in Fig. 11and Fig. 12, the power dissipated on the MOSFET has been evaluated by means of the plots of Fig. 13 and Fig. 14, where the time evolution of the dissipated power has been approximated with equivalent P*t discrete envelopes, to simplify the computation.

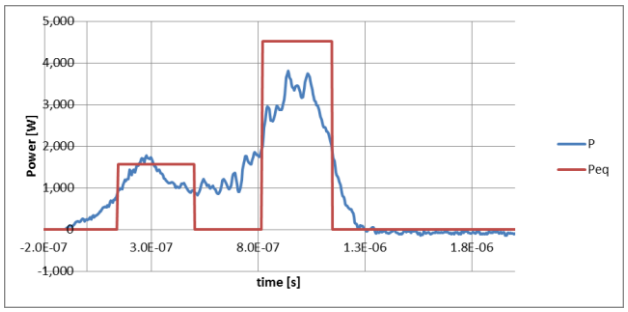

Figure 13. MOSFET power dissipation. Peak current.

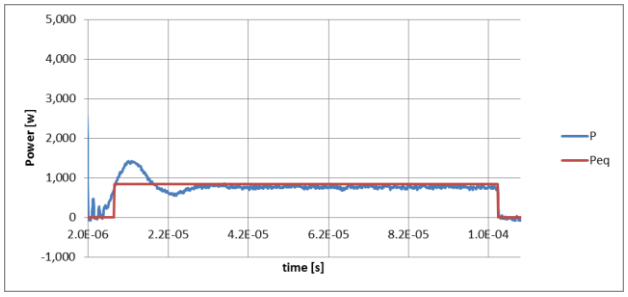

Figure 14. MOSFET power dissipation. Limitation.

Fig. 15 shows the thermal junction-to-case resistance of the FET has been extrapolated from the datasheet.

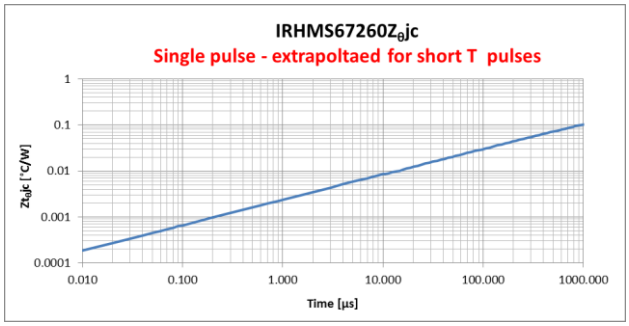

Figure 15. Single pulse thermal impedance versus pulse duration. Short pulses extrapolation.

A temperature rise of about 8°C results in the first (fast) transient (current peak of Fig. 13, about 1.2µs long).
During the nominal limitation (Fig. 14) a temperature rise of about 25°C resulted from the computation.
An overall temperature rise of about 33°C has been estimated at worst from both the simulations and measurements.
Considering a reasonable maximum mounting temperature that does not exceed 70°C, as it is in the specific application, the overall maximum junction temperature has been estimated not exceeding 103°C. This figure is well inside the derated value of 110°C, that is the acceptability level stated in para.§ 4.
It must be further considered that the intervention of the protection occurs only once in the operating life of the component, so that no accumulation of stress is foreseen.

6. UNLATCH FUNCTION

The limitation circuit output is latched into a Flip-Flop that disables (opens) the S3R MOSFET in case of activation. In normal operation the Flip-Flop is unlatched, leaving free to work (open, shunt, switch) the MOSFET.
An automatic un-latch mechanism has been designed to allow the recovery of unwanted spurious intervention of the latch protection.
This mechanism is driven by the error signal that controls the S3R function.
The reset is activated when the error signal exits its operating range upwards and meets a predefined threshold. When this happens too much power is delivered to the bus; the unlatch function triggers a command that resets the Flip-Flop and restores the normal operation of the MOSFET.
As every section has its own unlatch circuit, the full operation of all the S3R section is restored to regain the nominal operation.
In case of a section actually latched after a diode short circuit event, it is reactivated and soon re-latched due to a further intervention of the protection.
A test on EBB has been performed to verify the transients related to this event. Fig. 16 shows the recording of the two consecutive events: failure of diode in short and unlatch after 10ms. The delay time is representative of the reaction time of the error signal after the diode failure in the specific tested configuration.

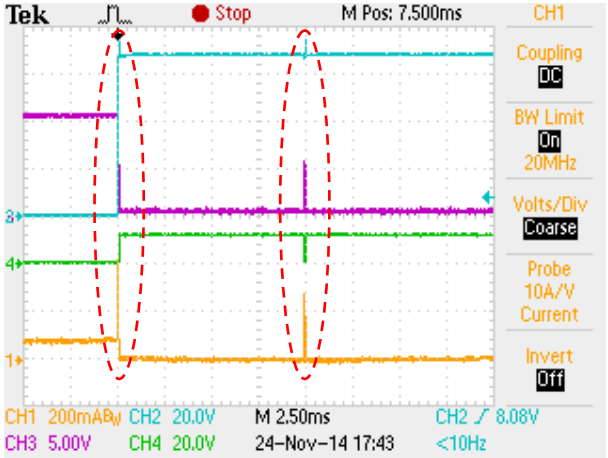

Figure 16. Un-latch after short of diode.

Fig. 17 and Fig. 18 show the zoom of the two transients of Fig. 16.
As expected the unlatch condition is less stressing, both in terms of peak current and of thermal stress, as the MOSFET is initially in "open" condition, so the first current peak results significantly lower.

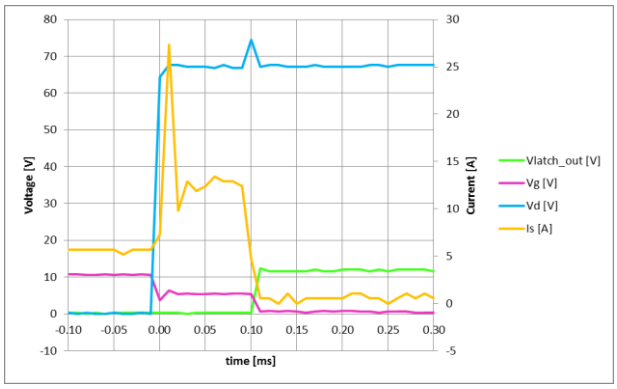

Figure 17. Diode short failure. 1st transient.

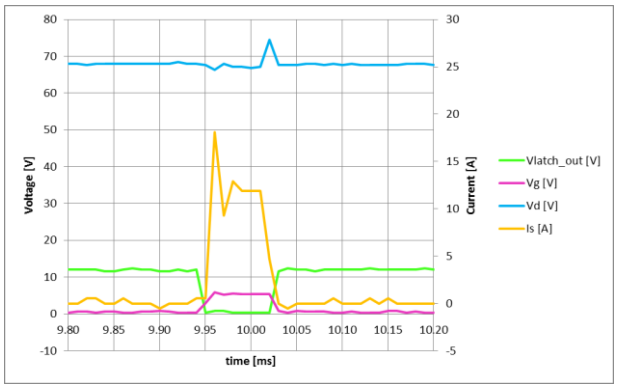

Figure 18. Un-latch event (and subsequent latch). 2nd transient.

The whole latch-unlatch electronics of the S3R section has been designed and verified to guarantee a correct initialisation at first power application. The correct initialisation of all the electrical parameters that concur to set the latch status is guaranteed by means of a delayed application of power supply to the electronics; the delay is obtained conditioning the release of the power supply to part of electronics and to FET driving circuit, by a threshold on the main internal supply.

7. S3R MODULE PHYSICAL REALISATION

The S3R concept described in this paper has been implemented for the first time in the frame of the earth observation program COSMO Second Generation.
The whole S3R function, made of 16 sections, has been allocated on two boards (8 per board) of reduced dimensions (about 240mm * 185mm), with a pace of 25mm between boards.
Fig. 19 and Fig. 20 show the top and bottom view of the S3R built for CSG PCDU.

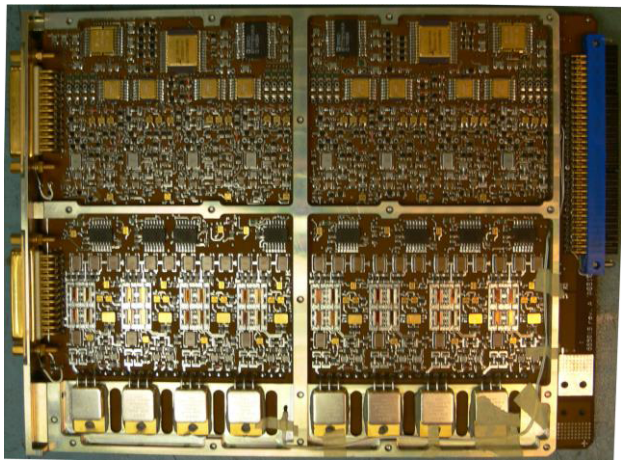

Figure 19. CSG S3R Top Side.

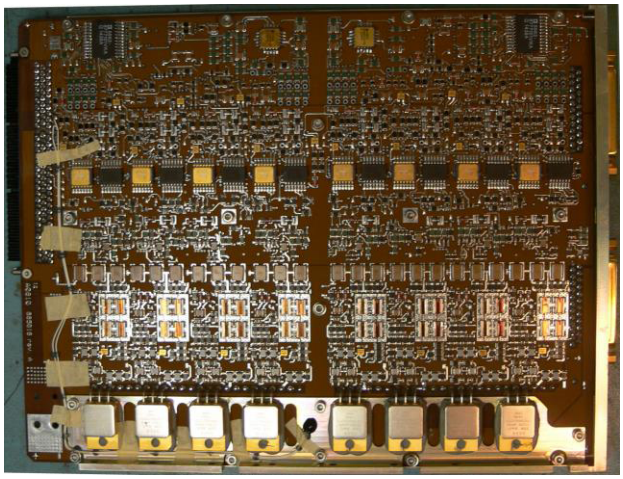

Figure 20. CSG S3R Bottom Side.

8. CONCLUSIONS

The feasibility of the proposed configuration for the S3R function has been demonstrated, meeting the electrical, thermal and reliability objectives.
The solution, deeply analysed, has been tested and validated on an EBB (complete for all the function) even at high and low temperature (in ambient pressure only).
The design has demonstrated, above all, its great advantages in terms of space occupation, as the electronics necessary to manage the main design aspects has been contained into acceptable dimensions, as the physical implementation clearly show.
As expected also the efficiency of the whole S3R has shown a really high figure (above 98%).

9. REFERENCES

[1] F. Tonicello, L. Bust Llavona, S. Keller "Synchronous Rectified, Single Diode Sequential Switching Regulator (S3R)", Proceedings of the 9th, European Space Power Conference, 2011.

10. ACKNOWLEDGEMENTS

A particular thank goes to Matteo Scrigna and Giorgio Ebale for their fundamental contribution in the definition and verification of the design of the solution presented in this paper.