

INTRODUCING THE RADIATION-HARDENED VOLTAGE REGULATORS RHFL4913 AND THE RHFL6000

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ABSTRACT

With the progressive scaling of the modern CMOS processes arising during the recent years, for the devices operating in space the susceptibility to the over-voltage events has increased. They have become more stringent the requirements in terms of accuracy of the supply voltage worth their reliability. For the case of CMOS memories operating at 1.5V it is essential to guarantee a variation of the nominal V_{OUT} to within 5% including those arising on the supply voltage during the transients.

Finally, for a voltage regulator operating in space one of the most salient effects are the voltage transients induced on the output by the single events (SET) that may exceed the aforementioned 5% threshold. This can be cause of damage into the circuitry fed downstream.

Among the devices in ST portfolio designed to cope with the mentioned effects there are two voltage regulators, the RHFL4913 and the RHFL6000.

The first one was initially developed for the harsh environment of the Large Hadron Collider. It was tested by the CERN and it was proven that it is able to operate without problems at up to 100Mrad TID at High Dose Rate without problems (1). Subsequent tests performed at low dose rates (expected in space environment), showed that this device is also ELDRS free up to 1Mrad (2). Further tests performed by NASA highlighted also a certain susceptibility to the SET (3) but this issue can be circumvented by the adoption of a properly sized up RC low pass filter put between the regulator output and the load as shown in fig.1 (4).

With the above provision, this regulator is suitable for operating in space. Currently, the RHFL4913 is QMLV qualified.

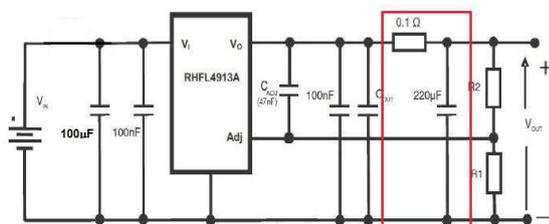
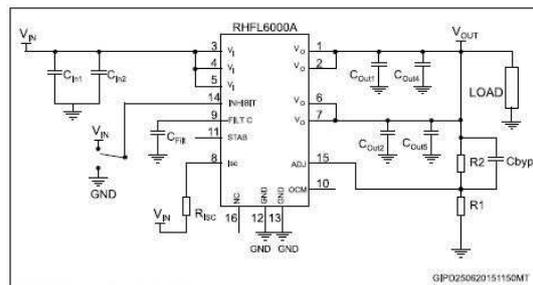


Figure 1 - Typical configuration recommended in space applications using the RHFL4913 with the RC filter (marked in red) for mitigating the Single Event Transients on the output

1. INTRODUCING THE RHFL6000

Nevertheless, a drawback of the filter mentioned above is the increase of the minimum $V_{IN}-V_{OUT}$ dropout needed for the regulation due to the presence of the 0.1Ω resistor in series to the output. In some applications, it would be preferable to gain efficiency by using a regulator capable of performing this action with the only capacitors used for the compensation at both input/output terminals. In this respect, the RHFL6000 can be considered an evolution of the RHFL4913. It was intended for circumventing the SET mitigation issue without need of any filter. By specific tests, it was seen that, with a combination of capacitors of proper characteristics put at both I/O terminals, a PCB configured as shown in fig.2 and with proper applicative rules it is possible to achieve SET of amplitude limited to within 3.3% of absolute V_{OUT} for up to 120MeV LET. Finally, this device is also QMLV qualified.



$C_{in1}=C_{out1}=C_{out2}= 47\mu\text{F}$ tantalum SMD ESR $\leq 60\text{mohm}$,
 $C_{in2}=C_{out4}=C_{out5}= 100\text{nF}$ SMD polyester
 $C_{filt}= C_{byp}= 22\text{nF}$ SMD polyester ; $R_{ISC} = 8.2\text{K}$ for $I_{sc}=2\text{A}$

Figure 2 - Pcb proposed for RHFL6000 with the recommended values for the components

For both regulators, pictures of the dices are given in figg.3 and 4 for RHFL6000 and RHFL4913 respectively.

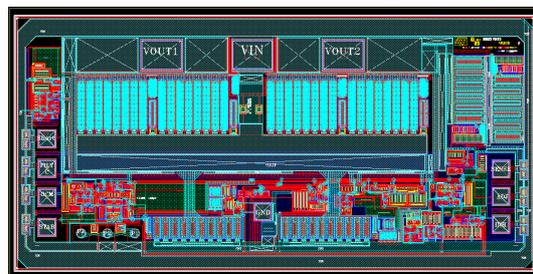


Figure 3 - RHFL6000 die

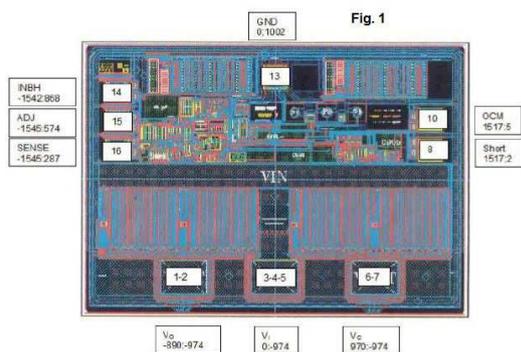


Figure 4 - RHFL4913 die

The immunity to radiation is achieved through a precise strategy involving the process selection and the definition of proper rules for both the design and the layout.

For what concern the first point, the ST process features high-speed bipolar transistors ($F_t = 6\text{GHz}$) intrinsically robust to the TID: tests performed at CERN at HDR showed a degradation of the β of 40% at 500Krad TID for both PNP and NPN. These bipolar transistors have an also relatively thin base (and this is, very likely, what makes these cells sensitive to the SEE).

As mentioned, the radiation immunity is achieved also through layout rules common to the rad-hard practice of design. These are intended to act against the parasitic effects induced into the single cells (one of these being the parasitic N-channels activated by the TID) by the extensive use of n+ ring into the NPN and PNP cells and the resistor pockets and p+ all over the dice.

A similar approach applies to cope with the Single Event Effects. On this subject, the layout of the pass element was also drawn by applying proper rules aiming at limiting the short transient current arising during the single events and causing peaks on the output proportional to the VIN-Vout dropout.

The basic layouts of the cells implemented are shown in fig. 5, 6 and 7 respectively for NPN, PNP and resistor pockets.

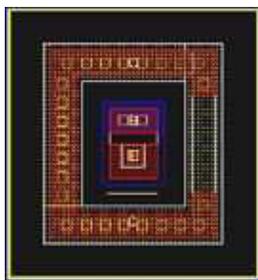


Figure 5 – NPN basic layout cell

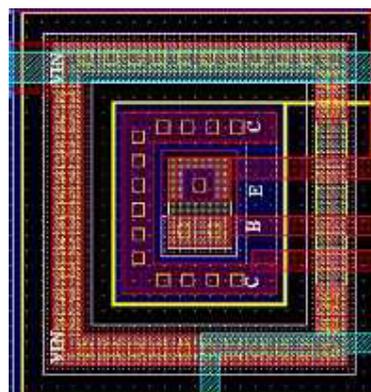


Figure 6 – PNP basic layout cell

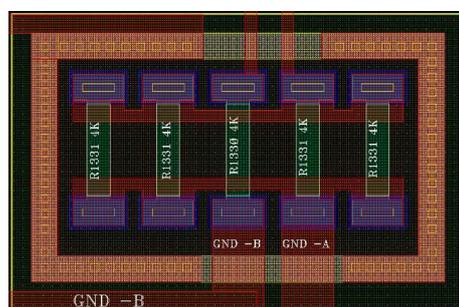


Figure 7 – Layout cell for Resistor pockets

Still on the TID provisions, at design level care also has been taken to set a minimum level of bias current to minimize degradation effects on the β and potentially bad operation of the regulator caused by the increased leakage.

In addition, both regulators are realized using only bipolar transistors which are known to be intrinsically more robust compared to their MOS counterpart.

Finally, for the SET immunity of the RHF6000, a proper feedforward scheme embedded (patent proposal is pending) switches ON during positive variations of the output voltage and provides a sinked current on the output (see Isinked in fig.8) contributing to the discharge of the bulk capacitor Cout.

This helps limiting the duration of the positive output transients and allows a fast recovery to the stationary regime of the regulator in a time shorter compared to a device with single ended output stage (fig.8). It turns helpful in case of long-duration SET induced.

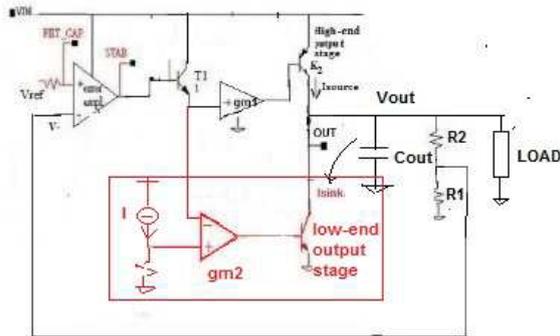


Figure 8 - RHFL6000: basic control loop architecture view

2. TECHNICAL SPECIFICATIONS AND EXPERIMENTAL RESULTS

As shown in TABLE1 the RHFL6000 is tested in accordance to the MIL-STD-883J Method 1019.9 in ELDRS conditions. For details regarding the TID tests, please refer to the table 1 [5]:

Table 1 - ELDRS Condition for tests on RHFL6000

Type	Conditions	Value	Unit
TID	50 rad(Si)/s high dose rate up to	300	krad
	10 mrad(Si)/s low dose rate up to ⁽¹⁾	100	
	ELDRS free up to ⁽²⁾	100	
Output voltage radiation drift	From 0 krad to 300 krad at 50 rad/s, MIL-STD-883J method 1019.9	<1.1	ppm/krad
Quiescent current (ON state)	From 0 krad to 300 krad at 50 rad/s, MIL-STD-883J method 1019.9 Vi = 2.5 V to 12 V, Io = 5 to 30 mA, Tj = -55 to +125 °C	<15	mA

For what concern the SET, the test were performed with the following bias configurations and trigger thresholds [5]:

Table 2 - SET: bias configurations and trigger thresholds

- For each configuration the parts were tested with the following bias conditions:
- Bias 1: VIN = 3V, VOUT=1.5V, Vinhibit=0V, IOUT = 1A, VINHIBIT = 0V,
 - Bias 2: VIN = 9V, VOUT = 0V, Vinhibit=9V, IOUT = 0A, VINHIBIT = 9V
 - Bias 3: VIN = 4V, VOUT = 2.5V, Vinhibit=0V, IOUT = 1A, VINHIBIT = 0V
 - Bias 4: VIN = 7V, VOUT = 5V, Vinhibit=0V, IOUT = 300mA, VINHIBIT = 0V
 - Bias 5: VIN = 9V, VOUT = 1.5V, Vinhibit=0V, IOUT = 100mA, VINHIBIT = 0V
 - Bias 6: VIN = 12V, VOUT = 9V, Vinhibit=0V, IOUT = 300mA, VINHIBIT = 0V

Trigger thresholds for SET test are defined, according to the bias conditions, in the following table:

	Bias 1	Bias 2	Bias 3	Bias 4	Bias 5	Bias 6
Vcc	3V	9V	4V	7V	9V	12V
Vout	1.5V	0V	2.5V	5V	1.5V	9V
Upper trigger threshold	1.55V	0.1V	2.58V	5.15V	1.55V	9.27V
Lower trigger threshold	1.45V	-	2.43V	4.85V	1.45V	8.73V

Results and conclusions are summarized in tables 3, 4, figs. 9 and 10 [5].

Table 3 – RHFL6000: SEL/SET Performances

Feature	Conditions	Value	Unit
SEL/B performance	LET = 120 MeV*cm ² /mg Vi = 12 V	No Latchup/burnout	-
SET performance during events	LET = 32 MeV*cm ² /mg Saturated cross-section = 6.18*10 ⁻⁵ cm ² Viu up to 9V Vi - Vo ≤ 7.5 V Iour < 300 mA	± 15% max over less than 300 ns	% of Vo
	LET = 120 MeV*cm ² /mg Viu up to 12 V Vi - Vo < 3.0 V Iour < 300 mA	No SET above ± 3%	
	LET = 120 MeV*cm ² /mg Viu up to 4 V Vi - Vo < 1.5 V Iour < 1 A	No SET above ± 3.3%	

Table 4 - RHFL6000: SET Cross Section

7.3.5.1. SET Cross sections

LET Eff (MeV.cm ² .mg ⁻¹)	SET Cross Section (cm ²)			
	N° 9	N° 10	N° 11	N° 12
120	3.00E-06	4.20E-05	6.20E-05	5.40E-05
102.8	1.00E-06	1.30E-05	3.25E-05	3.05E-05
86.37	2.00E-06	8.00E-06	2.70E-05	2.40E-05
70	<1.00E-06	8.00E-06	2.30E-05	2.05E-05
60	<1.00E-06	9.33E-06	3.40E-05	3.35E-05
46.5	<1.00E-06	<1.00E-06	1.30E-05	1.50E-05
32.3	<1.00E-06	<1.00E-06	<1.00E-06	<1.00E-06

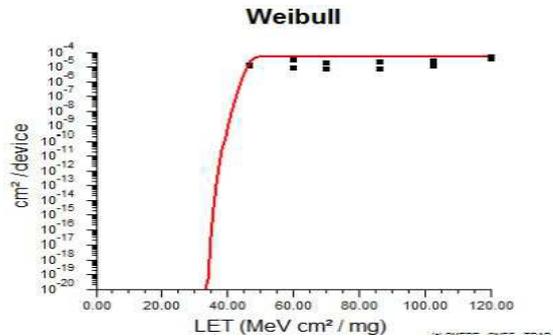


Figure 9

The main objective of this test was to evaluate the sensitivity of the RHFL6000, a Rad-Hard Voltage Regulator to Single Event Latch up (SEL) and Single Event Transient (SET).

The irradiation was performed at RADEF with a maximum LET at 120 MeV.cm²/mg.

The mains conclusions are the following :

- No SEL was observed up to LET of 120 MeVcm²/mg and up to temperature of 125 °C.
- No SET was observed on bias 1 to 4 and 6
- SET was observed in bias 5 (VIN= 9V, VOUT= 1.5V, IOUT= 100mA, VINHIBIT= 0V).

The LET threshold was 32.3 MeV.cm²/mg with a saturation cross-section of 6.18E-5 cm²

Figure 10

During these experiments, the trigger threshold for SET detection was set a 3.3% of the absolute value of VOUT.

It is worth noticing that, of all the configurations bias under examination, SET exceeding the mentioned target were detected only on the one labelled as bias 5. The corresponding LET threshold was 32.3MeV*cm²/mg and the saturation cross section 6.18 e-05 cm².

The worst case SET observed is shown in fig.11

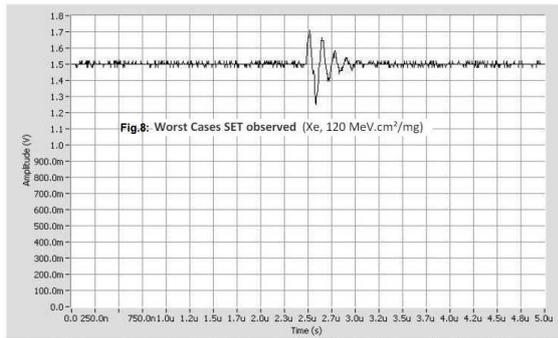


Figure 11 - RHFL6000: SET Worst Case

The standard performances can be summarized into the table below:

- Input voltage range from 2.5V to 12V
- 2A guaranteed output current
- Low dropout: 0.3V typ. @ 0.4A
- Embedded over-temperature and overcurrent protection
- Adjustable overcurrent limitation
- Output overload monitoring/signalling
- Adjustable output voltage
- Internal control loop accessible via an external pin
- Inhibit (ON/OFF) TTL compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Rad-hard: guaranteed up to 300krad
MIL-STD-883J Method 1019.9 high dose rate and 0.01 rad/s in ELDRS conditions
- Radiation environment: SET/SEL/SEB:
 - SEL free @ LET=120MeV*cm²/mg
 - SET: less than 3.3% of V_{OUT} @ 120MeV
- Heavy Ions SET dedicated internal circuitry implemented for absorbing output transient
- Operating junction temperature range: -55°C to +125°C

3. ADDITIONAL FEATURES OF THE RHFL6000 STABILITY

In order to comply with the requirement of the 5% absolute max target of V_{out} during a transient, it was seen that it is essential that the regulator operates with capacitors, at both I/O, having the following constraints: C_{out} >= 100μF; ESR <= 30mΩ. This means that the regulator must be stable with these capacitors. In some applications, the mentioned condition can lead to stability margins not compliant with the targets in space. One of these cases is when a load supplied at the output

is too low. In this case, it is possible that the zero brought by the output capacitor is not sufficient to increase the phase near the cutoff frequency Ft because located too far from it. To overcome this issue, in the RHFL6000 design it was considered the possibility of adding a further external zero Z_L, close to Ft, using the classical lag compensation approach. By inserting an RC group between the terminals CSTAB and GND, if such zero falls within one decade left to Ft, it can provide a positive phase shift to the Bode diagram and the phase margins are thus increased. To achieve this effect, one must consider that an external RC group in that location adds also a pole P_L left to the zero. If the P_L/Z_L ratio is not adequately calibrated, the negative shift of P_L can compensate that of Z_L. Therefore, it is fundamental to determine a convenient ratio for the doublet (P_L,Z_L) to avoid this effect. In this respect, a model compatible with Pspice is made available by ST with which it is possible, starting from the application data, to determine Ft and optimize the mentioned external impedance.

For a generic series RC group with an impedance R_o in parallel we have

$$P_L = 1 / [2\pi (R + R_o)] \quad (1)$$

and

$$Z_L = 1 / (2\pi RC) \quad (2)$$

For the RFL6000, R_o is the dc impedance seen at the output of the error amplifier and is ≅ 1MΩ @ T=25V

Therefore,

$$P_L / Z_L = R / (R + R_o) \quad (3)$$

Concerning the main poles and zeroes determinant for the stability, with reference to the general LDO scheme in fig.12, we have

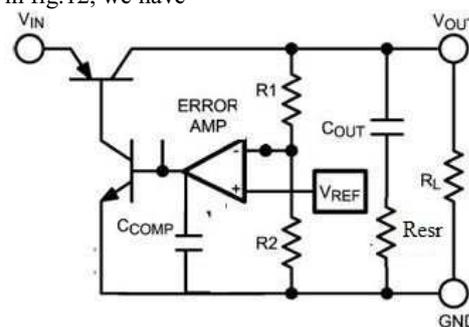


Fig. 12: Basic scheme of an LDO

$$P_o = \frac{1}{2\pi R_{out} C_{out}} \quad (4)$$

and

$$Z_o = \frac{1}{2\pi Resr C_{out}} \quad (5)$$

where:

Rout = impedance seen between Vout and GND, given by the parallel combination of the load RL with the resistor divider couple R1+R2;

Resr= series resistance associate to the output capacitor Cout.

There is also an internal pole, Pint, located at the output of the error amplifier. For the RHFL6000, Pint ≅ 800 Hz.

An applicative example of the achievable result is shown in fig. 13. Application conditions are:

Vin=5V Vout=2.5V; RLOAD=250ohm, Cout=220µF, ESR=30mΩ, R1=R2=10KΩ.

In this example, Ft=24Khz, ZL was set at 10khz and PL at 9Khz, that is away on the right from Pint.and Po. This was achieved with an RC group Cp=300pF, Rp=160Kohm. Notice the increased phase near to Ft

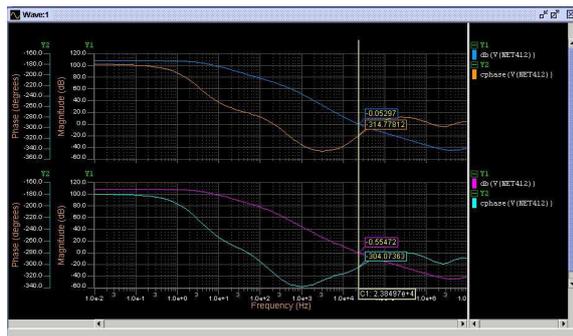


Figure 13: Effect, on the Bode diagram, of an RC series group (R=200KΩ, C=300pF) put between CSTAB and GND.

About the impact on the transient response accuracy, relevant plots are shown in fig.14.

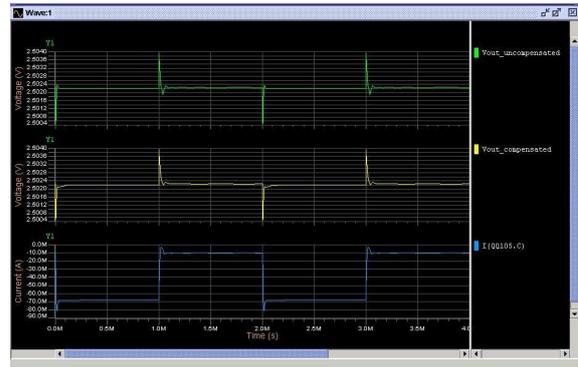


Figure 14: Effect of the added RC group on the load transient accuracy of the RHFL6000 with the RC group between CSTAB and GND inserted (yellow) and the same group unconnected (green).

4. CONCLUSIONS

The RHFL6000 is a regulator showing high performances in terms of immunity to the TID absorbed and to the Single Event Effect.

Tests showed that, with a proper configuration PCB, part selection and applicative guidelines this regulator is suitable for sourcing the supply voltage to devices requiring a tight control of the supply voltage amplitude, such as the 1.5V FPGA memories, microprocessors and other devices realized into the modern submicron CMOS process.

5. REFERENCES

- (1) Radiation performances of the L4913 voltage regulator, N. Boetti, P.Jarron, B. Kisielewsky, F. Faccio , Radiation Effects Data Workshop, 2002 IEEE Conference Publications
- (2) Evaluation of STMicroelectronics RH-L4913 Positive Hardened low drop voltage regulator. P. BRIAND, STMicroelectronics, Marielle BELASIC,CNES, Jean-Francois VADROT, STMICROELECTRONICS, 2002
- (3) SEE test Report V.1.0 Heavy ions SEE test of RHFL4913 from STMicroelectronics, Christian Poivey, Hak Kim, Anthony Sanders, NASA Jan. 23, 2006 - T121805_RHFL4913
- (4) SEE test Report V 3.0 Heavy Ino test of RHFL4913 from STMicroelectronics with SET mitigation circuitry, Christian Poivey, John Pandolf, Anthony Sanders, Hak Kim, Sept 19, 2007
- (5) TRAD - HEAVY IONS TEST REPORT Single Event Effects RHFL6000 Sept. 23, 2014

- (6) Relationship between frequency response and settling time of operation amplifiers - by Yeshwant KAMATH, Robert MEYER, Paul GRAY, IEEE JSSC, dec 1974