DIGITAL CONTROL FOR POWER MANAGEMENT SYSTEMS

Bekemans Marc [(1)], Acconci Terence [(1)] , Van Humbeeck Thierry [(1)] , Van Esbeen Alain [(1)]

[(1)] Thales Alenia Space Belgium, Rue Chapelle Beaussart 101, B-6032 Mont-sur-Marchienne, Email: firstname.name@thalesaleniaspace.com

ABSTRACT

The present document aims to show the advantages of a digital implementation of the regulation(s) used for the control of DC/DC converters. In a first step, a general overview of the capabilities provided by digital solution, w.r.t. analogue, will be introduced. An example of a pure digital algorithm (the predictive programmed current control) will also be presented. In a second step, a practical application of a digital control will be considered. In this example, the output voltage of two Buck DC/DCs, connected in parallel, is controlled via a digital regulation. This application also integrates different possible features (soft start, current sharing, embedded scope…), easy to implement in digital, and whose analogue equivalent would be hard or impossible to obtain. Finally, a quick overview of the radiation-hardened ASIC developed by Thales Alenia Space will be given. This component, called "Digital Programmable Controller" (DPC) is totally suitable to implement digital regulations for space applications.

1. DIGITAL REGULATION CONCEPT

1.1. Introduction

The introduction of digital regulation in power converters is a good opportunity to imagine new concepts of regulation. We will first expose several way to "digitalize" classical control principle like : Peak Control, PWM Control, and Hysteresis Control. And finally present a pure predictive controller which is only realizable by digital processing and not be limited by the classical stability criterion liked to the phase lack due to calculation time.

1.2. Digital "equivalent" to analog regulations

Current average mode (CAM)

Current average mode (CAM) regulation algorithm is one of the most common inner-and-outer-loops regulation systems. The principle here is to use an inner current loop which will regulate the average current in the inductance of the converter. The reference average current will be provided by the outer voltage loop, which will be in charge of regulating the output voltage. As illustrated in Figure 1, the output measured voltage is compared to a reference voltage, and the error goes into a first regulator. This regulator provides an average current reference which will be compared to a measured average current, giving a current error which will be processed into a second regulator to give a duty cycle to apply to the Buck system.

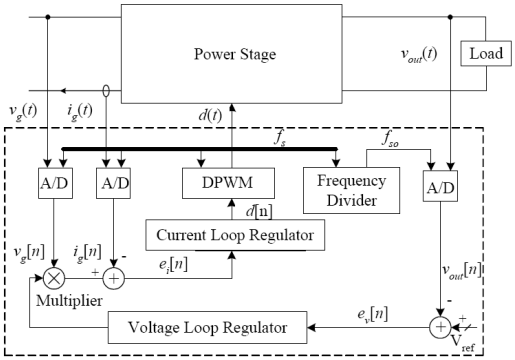

Figure 1 : Current average mode regulation

Current peak mode (CPM)

Current peak mode principle is almost the same than for the current average mode, except that here, only one regulator will be used. The output measured voltage is compared to a reference voltage, and this error goes into the regulator. This one provides the maximum current that the inductance current of the Buck has not to exceed. This maximum current reference is compared to the measured current through an analog comparator, and the result drives the "reset" input of a RS flip-flop, which cuts the transistor of the switching power system, making the current into the inductance decrease.

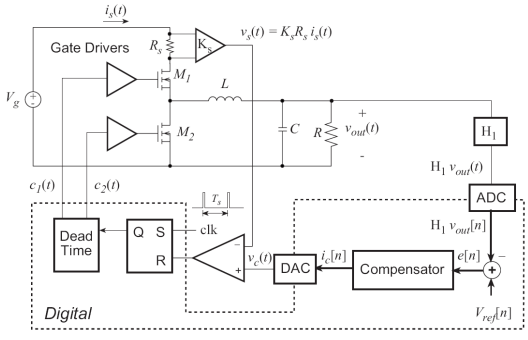

Figure 2 : Digital implementation of current peak mode

It is important to note that the current amplifier, comparator & flip-flop are all components of the analog chip and that the analog was foreseen such as to be the "analog components" of a current peak mode regulator.

1.3. Novelty : Digital Predictive Controller

These two methods (digital current average mode & digital current peak mode) have been successfully tested. However further thoughts lead us to conclude that this approach was a bad copy of analog implementation.
Everyone agrees that the digital technology brings more flexibility, more versatility, more stability of the parameters…but everyone also contends that the price to pay is a reduction of dynamic performance due to calculation time and sampling delay. It is, indeed, generally the case but in switching converters a predictive controller could take into account the sampling time due to switching and reach dynamic performance very close to that of peak control even if we sample the output signal only once per switching period. The leitmotif in digital design is: don't transpose to digital what is being done in classic analogue circuits. The search for improvements brings us to distinguish two different axes on which we can work:

- **Improvement of dynamic response** of algorithm in order to be as good as analogue controller in small-signal dynamic but better in large signal or in non-linear operation.
- **Improvement of observability**, for two reasons: the first is the improvement of the "knowledge" necessary to achieve a more effective control, the second is that the digital concept could help us to reduce the number or the performance of sensors by numerical reconstruction of state variables.

The dynamic response is linked to the bandwidth capability of the system under the constraint of conserving the stability margin. A fully digital predictive peak controller could avoid the problem of stability but transpose peak control to digital is difficult because the "off" decision is made on a cross value criterion. That means we need an a comparator to define the ON-OFF transition. Another way is to implement the recurrent equation of "peak control" in a numerical form and let it work on a sampled value. We cannot speak any more in that case of peak current control; we shall rather call it Programmed Current Control (PCC) but the dynamic performance is kept. These alternatives are summarized below:

Digital PID Controller

- carries over the drawbacks of average current control
- has an additional delay due to sampling and the computation time. This reduces the dynamic of the control
- seems difficult to perform as well as the analog solution
- exploits the advantages of digital for adaptive parameterization of the corrector

Predictive Programmed Current Control:

- carries over the advantages of Peak Current Control
- Doesn't use an external analog comparator
- Reserves one switching period for computation
- Only uses one current sample per switching period.

In analog it's possible to control only the valley or the peak because the "measurement" instants (crossing of the "off" threshold) are simultaneous to the "action" instants. With a digital system, any point of the current sequence can be sampled. This can be done by synchronizing the sampling time with the PWM sequence. The consequence is that we could regulate any intermediate value between peak and valley.

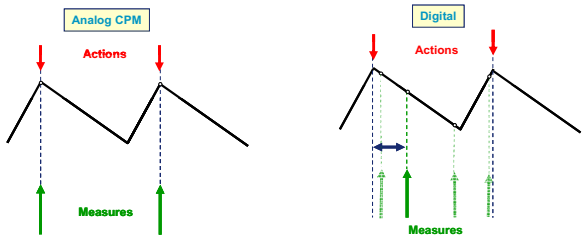

Figure 3: Digital controller could regulate any point between peak and valley

With the assumption of reacting within one switching period to any perturbation, the mathematical analysis of the recurrent system yields the following recurrent equations which links the duty cycle and the current. The variables m_1 and m_2 are respectively the rising and falling slope of the current; me_1 and me_2 are the estimated rising and falling slope set into the corrector. Let us notice that this form is usable for any topology: only the definition of m_1 and m_2 changes. Example for à Buck:

$$m_1 = \frac{V_{in} - V_{out}}{L} \qquad m_2 = \frac{-V_{out}}{L}$$

The Recurrent Equation of the Predictive Programmed Current Control are:

$$\mathbf{X}_{n+1} = \mathbf{A} \cdot \mathbf{X}_n + \mathbf{B} \cdot \mathbf{U}_n \tag{1}$$

With:

$$\mathbf{X}_n = \begin{bmatrix} I_n \\ \theta_n \end{bmatrix} \qquad \mathbf{U}_n = \begin{bmatrix} 1 \\ I_{ref} \end{bmatrix} \tag{2}$$

$$\mathbf{A} = \begin{bmatrix} 1 & (m_1 + m_2) \cdot Ts \\ \dfrac{-1}{(me_1 + me_2) \cdot Ts} & -1 \end{bmatrix} \tag{3}$$

$$\mathbf{B} = \begin{bmatrix} -m_2 \cdot Ts & 0 \\ \dfrac{2 \cdot me_2}{(me_1 + me_2)} & \dfrac{-1}{(me_1 + me_2) \cdot Ts} \end{bmatrix} \quad (4)$$

This equation materializes into the following block diagram where the structure is independent of the topology: only the internal gain has to be adjusted to the power topology used. It's interesting to see that we recover all feed forward effect naturally present in Analog Peak Current Control.

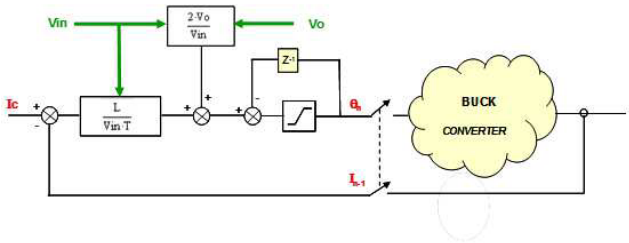

Figure 4: Control block diagram of predictive Programmed Current Control for a Buck converter

This approach is completely different from that of classic control. To convince ourselves, let us look at the loop gain: it is equal to one for all frequencies. This is not a feedback system! Indeed, in feedback systems we replace the lack of knowledge by the gain. Here, the loop gain is 1 for all frequencies! This is a pure predictive controller without analog equivalent.

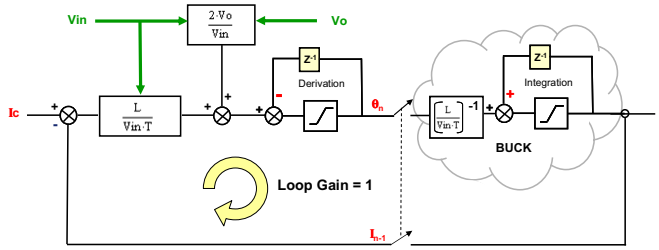

Figure 5: Control block diagram of predictive Programmed Current Control

2. APPLICATION OF DIGITAL PROCESSING : DIGITAL CONTROL OF POLYPHASE PARALLEL BUCKS

Plenty of applications for DC/DC regulation can be imagined using a digital regulation. Indeed, once the different measurement are digitalized using ADCs, they can be combined in many different ways, in order to achieve the expected regulation functionality and performance. This makes a strong difference w.r.t. an analogue regulation, and this is what the application developed in the current paragraph aims to show.

The hardware of this application is the following : two Bucks DC/DC connected in parallel to a single external load, and whose output voltage is regulated thanks to a digital regulation. In practical, the DPC component (see paragraph 3) was used and placed on its DPC Reference Kit.

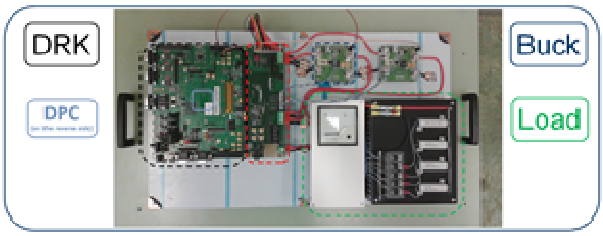

Figure 6 : Digital control of polyphase parallel Bucks : hardware view.

The next paragraphs aim to show the different functionalities that were implemented here.

2.1 Embedded scope feature

Plenty of different measurement were implemented, like input and output currents/voltages of both DC/DCs. In order to be able to easily follow the evolution of all these measurements, an embedded scope feature has been implemented. All the measurements are stored and can be displayed, on demand, on several graphs. Here, not less than 6 measurements were retrieved in the same time. This kind of embedded scope is a strong advantage of the digital. With an analogue regulation, several oscilloscopes, with synchronisation between them, would have to be used to achieve the same result. In addition, it is important to note that not only measurement can be retrieved via this feature, but also any digital variable used in the algorithm (for instance the calculated duty cycle, or any required variable useful for debug purpose). *Figure 7* to *9* illustrate the results obtained via the embedded scope.

2.2 Soft start

During the start-up phase, the output capacitance is charged, leading to a potential high in-rush current at the input of the DC/DC converter. This can be handled by using a soft-start control algorithm, smoothing the initial duty cycle evolution in order to control the in-rush input current. This is illustrated in *Figure 7*, where we can see that the input current ("Iin") and the output current of the Bucks ("IoutA", "IoutB") are controlled. The soft start parameters (duration, slope of the current) can easily be changed on-line, by only modifying some digital parameters in the regulation code.

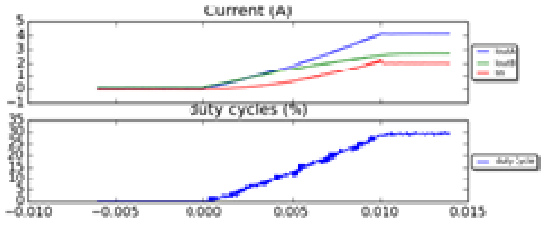

Figure 7 : Soft start behaviour.

2.3 Output current sharing

The output current of both Bucks are measured. This information can be used in order to tune the regulation to achieve a perfect current sharing at the output of both Bucks. This is illustrated in *Figure 8*, showing what happens when the current sharing algorithm is activated, starting from an initial condition where both Bucks are strongly unbalanced.

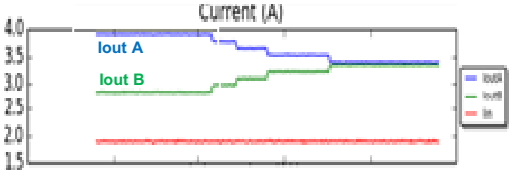

Figure 8 : Activation of the output current sharing algorithm.

2.4 Activation/deactivation of the second Buck

Using two Bucks in parallel has several advantages : on one hand, the maximum power provided to the output load can be higher, on the other hand the output ripple can be smaller, if both Bucks are used in a polyphase way (i.e. with the PWM signal shifted by one half of the switching period from one Buck to the other). In addition, the load transient performance will be better (because each Buck only "sees" one half of the current transient). However, using two Buck in parallel can lead to dramatic loss of DC/DC efficiency if the output current is too small. A simple way to avoid this phenomenon is too deactivate the second Buck if the output current becomes too small, and to reactivate it when the output current is increasing. This kind of algorithm is quite simple to implement in digital. It can also easily be re-configured (e.g. change of output current threshold, implementation of hysteresis), or adapted. For instance, we could imagine another criterion based on the DC/DC efficiency, computed from the voltage and current measurements performed at the input and the output of the DC/DCs. Figure 9 illustrates what happens when one Buck is deactivated.

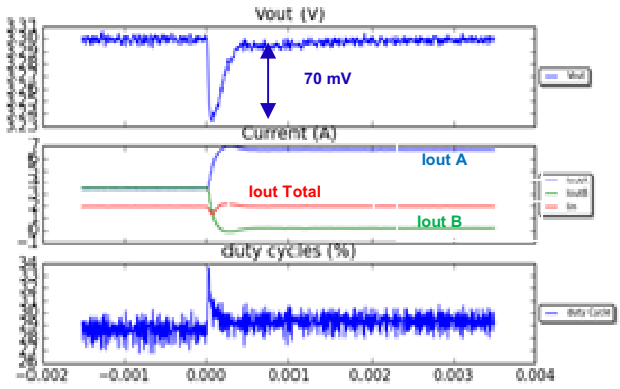

Figure 9 : Deactivation of one Buck

2.5 Regulation algorithm

The output voltage regulator implemented here is a PID. Since it is a digital regulation, the parameters of the regulator can easily be changed, in order to tune the regulation bandwidth, the recovery time,… Additional features can also be added, like saturations, slew rates, or measurement pre-processing (e.g. median on successive samples). All these elements are easily implementable in digital. In addition, more advanced algorithm can be considered, like the predictive algorithm presented in paragraph 1.3 (and in [1]), involving three different measurements, and including the processing time in its definition. Other algorithms, like sliding mode control ([2]), capacitor charge balance ([3]) or additional feed-forward ([4]) could also be considered. In the end, the easy tuning of the algorithm parameters as well as the possibility of using more evolved algorithms are strong assets of the "digital world".

3. DIGITAL PROCESSING IMPLEMENTATION

3.1 Implementation means needs

Digital power control tasks require signal digital acquisition (ADCs), signal digital processing, and PWM generation functions. Some auxiliary functions are often required, like protection, soft start, telemetries & tele-commands (TM/TC) handling via a data communication interface, signal observation capabilities, …

From performance point of view, the following parameters are critical: the ADC conversion and digital processing latencies, and the ADC & voltage reference accuracies. The first will determine the regulation bandwidth (a few µs maximum), the second will determine the residual error (typically a few tenth of percent maximum).

3.2 Implementation targets

Given the needs introduced in previous section 0, digital functions can be targeted in an FPGA, with peripheral ADCs, reference voltage source, and oscillator. For space applications, those components shall be radiation hardened, leading to high components bill of material (BOM).
To overcome this cost problem, Thales Alenia Space takes benefit of the Digital Programmable Controller ("DPC") ASIC, which embeds all required functions in the same radiation hardened component, at a much cheaper BOM.

3.3 The Digital Programmable Controller ("DPC")

The DPC ASIC (see *Figure 10*) is a radiation hardened mixed-mode and multi-core micro controller, developed in the frame of an ESA ARTES program. It targets DC/DC converter control applications, together with

other applications like motor control, general purpose analog & digital TM/TC interface on CAN or MIL-1553B buses, intelligent sensor management, monitoring and protection.
The DPC architecture is shown on *Figure 11*. For power management functions, a regulation arithmetic sequencer running at 40 MHz handles digital power control tasks. It includes 4 low latency (1µs) 13 bits accurate ADCs, multiplexed to 16 inputs. Those inputs are processed by a dedicated 16 bits micro controller core with multiplication & division functions (in red on *Figure 11*). The control feedback action is applied via up to 6 complementary PWM outputs clocked at 120MHz, and up to 3 linear analog outputs (DACs).

The ASIC embeds its internal power supply LDO, an accurate voltage reference, and a frequency reference. Besides the regulation core, three other micro-controller cores are assigned to respectively TM/TC communication tasks (in green on *Figure 11*), supervision tasks, and activity and signal observation tasks.

The circuit is radiation hardened: >60krad(Si), SEL LET_{th} >68 MeV.cm²/mg, SEU LET_{th} >40 MeV.cm²/mg. The performances are guaranteed in the -55°C to +125°C temperature range.

Figure 10: the DPC ASIC

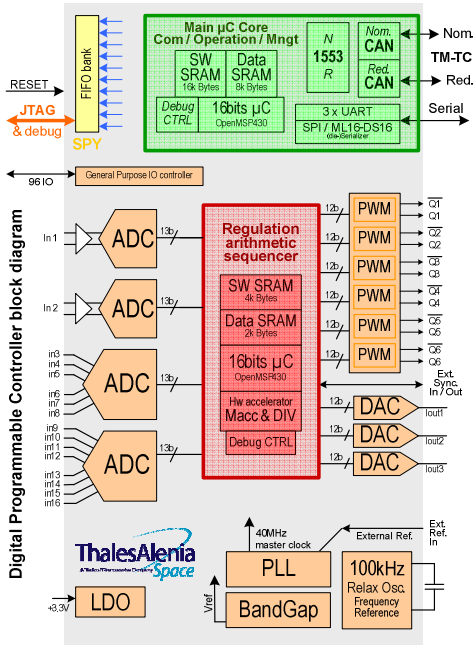

Figure 11: DPC block diagram

The circuit is fully validated since 2015, and is already used in Thales Alenia Space observation and telecom equipments.

3.4 Rapid prototyping and FM implementation

Besides the DPC component, Thales Alenia Space has developed software and hardware toolkits that allow fast prototyping any power controller.

For instance, the DPC Reference Kit (DRK) is a hardware board that implements the DPC and all its signal interfaces. Once connected to a development laptop via USB, and to power components, it allows application engineers focusing on the design of the controller algorithm.

The DPC Plugin Module ("DPM") is an FM grade mezzanine board that contains the DPC chip and some auxiliary circuits like CAN transceivers, APS and LCL. Once plugged on the application power hardware (FM), it is ready to be programmed with the power controller (or any other application). This approach drastically reduces implementation and integration costs.

4. CONCLUSION

Today, all the required elements are available to handle the digital control for power converters. Indeed, suitable digital algorithms as well as a dedicated component compatible with space environment exist. These elements have been included in a DC/DC demonstrator and are now ready to be part of future space power products.

5. REFERENCES

1. J. Chen, A. Prodic, R.W. Erickson, D. Maksimovic (2003). Predictive Digital Current Programmed Control. IEEE transactions on Power Electronics, vol. 18, no. 1, 411-419
2. E. Vidal-Idiarte, C.E. Carrejo, J. Calvente, L. Martinez-Salamero (2011). Two-Loop Digital Sliding Mode Control of DC-DC Power Converters Based on Predictive Interpolation. IEEE transactions on Power Electronics, vol. 58, no. 6, 2491-2501
3. G. Feng, W. Eberle, Y-F. Liu (2007). A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters. IEEE transactions on Power Electronics, vol. 22, no. 4, 1489-1498
4. S. Chae, B. Hyun,W. Kim, and B. Cho (2008). Digital load current feed-forward control method for a dc-dc converter. APEC 2008 - Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 498-502.