Development of Intelligent Building Energy-saving Temperature Control System Based on FPGA

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Abstract. The ideal energy-saving building should meet the environmental quality of living space in different seasons with the least energy consumption. The indoor temperature of the building is an important consideration. However, most temperature control systems have certain problems. In order to improve the stability and accuracy of the temperature control system, a system based on FPGA+Verilog HDL for intelligent adjustment of indoor temperature is designed. The purpose of the system design is to achieve the dual effect of comfortable and energy-saving living environment. The system uses an integrated temperature sensor DS18B20 as a temperature sensing element. FPGA as the master control center to process data. The system is programmed with the hardware description language Verilog HDL. The temperature control system uses a digital PID control algorithm. The simulation results verify the correctness of the design.

1 Introduction

The ideal energy-efficient buildings should meet the environmental quality of living spaces in different seasons with minimal energy consumption. The main ways of building energy conservation include: reducing the energy loss of building envelopes; reducing the energy consumption of building facilities; minimizing the consumption of non-renewable energy and improving the efficiency of energy use. In these aspects, high technology plays a decisive role. This paper designs a system based on FPGA that uses the serial port to transmit data, which can intelligently adjust the indoor temperature. It not only maintains the comfort of living, but also saves energy, achieving the dual effects of comfort and energy saving.

Setting the temperature range, temperature control beyond the set allowable range is a common temperature control method. This method is simple to implement and low in cost, but the temperature control accuracy is not high, and the time to reach the stable point is long. Therefore, it can only be used in occasions where the accuracy is not high. The temperature control system designed in this paper adopts digital PID control algorithm, which can freely set indoor temperature within a certain range. The temperature fluctuates within $\pm 1^\circ\text{C}$ under steady state. It has high control precision and can overcome capacity lag. It is suitable for control energy-saving aspects of smart buildings with high quality requirements. Using FPGA to realize the design of temperature control system can not only improve the computing speed of the system, reduce the volume of the system, but also enhance the reliability of the system, and has a strong application prospect.

2 System overall design

The overall design block diagram of the system is shown in Figure 1. The front stage of the temperature control system uses the DS18B20 model temperature sensor for temperature measurement, and then is amplified by the preamplifier and sent to the analog/digital converter to sample and analyze the obtained digital signal, automatically select the appropriate PID coefficient and calculate the corresponding duty cycle coefficient of the heating (or cooling) waveform. The DDS built by the FPGA reads the corresponding duty cycle and converts it into a waveform output, sends the corresponding control signal, and infrared controls the air conditioner, thereby achieving automatic temperature control and achieving the purpose of building energy saving.

Fig. 1. System overall design block diagram

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3 System hardware design

3.1 Pre-sampling circuit

The DS18B20 is a single-wire digital temperature sensor manufactured by DALLAS. One of its greatest features is the use of single-bus data transmission. It integrates semiconductor temperature sensitive devices, A/D converters, memories, etc. on a small circuit chip, and the sensor directly outputs the complement of the digital value of the temperature signal. Real-time temperature detection and display with the DS18B20 enables fast measurement of ambient temperature and strong electromagnetic immunity, which can adapt to more complex and harsh working environments with high reliability.

The DS18B20 temperature sensor has 1 pin grounded, 2 pin is used as the signal line, which is connected to the corresponding pin of the FPGA. The 3 pin is connected to the power supply, and the display circuit uses the LCD screen. Temperature measurement range is $-55^{\circ}\text{C} \sim +125^{\circ}\text{C}$, programmable 9-bit to 12-bit A / D conversion accuracy, temperature resolution up to 0.0625°C , the measured temperature is extended with a 16-digit number string line output, DS18B20 temperature data table is shown in Table 1. According to the development data of the temperature sensor, the running state machine programs the temperature sensor, and operates the DS18B20 in three steps: initialization, ROM command, and function command.

Table 1. DS18B20 temperature data

Temperature	Digital output(Binary)	Digital output(Hex)
+110°C	0000 0110 1110 0000	06E0h
+70°C	0000 0100 0110 0000	0460h
+15.0625°C	0000 0000 1111 0001	00F1h
+5.125°C	0000 0000 0101 0010	0052h
+0.5°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1111 1000	FFF8h
-5.125°C	1111 1111 1010 1110	FFAEh
-15.0625°C	1111 1111 0000 1111	FF0Fh
-70°C	1111 1001 0010 0000	F920h

3.2 Data display circuit

The temperature value is displayed by a seven-segment LED with the common cathode. Four digital tubes are required to display the temperature value set by the keyboard and the measured temperature value. Because the four digital tubes occupy more I/O port resources of

the FPGA, the integrated display decoder CD4511 with drive and latch function is used. As shown in Figure 2, a digital tube is connected to the FPGA. The display of the set value and the measured value of the Verilog HDL programming are displayed in two different modules.

Fig. 2. Digital tube and FPGA connection

3.3 FPGA hardware

FPGA is the core of the temperature control system design. Its system structure is divided into five parts: user interface, clock generator, PID controller, PWM wave generator and sensor interface. This system uses DIGILENT's Nexys A7-100T chip. The Nexys A7-100T chip has a total of 15850 logic slices, each with 4 6-input LUTs and 8 flip-flops, 4860Kbits of fast RAM. It has six clock management modules, each with a phase-locked loop (PLL), 240 DSP slices, analog-to-digital converter (XADC). Compared to earlier versions, the optimized Artix-7 FPGA chip enables higher performance logic, better performance, and richer resources to meet the needs of this system design. The internal structure of the FPGA is shown in Figure 3.

Fig. 3. FPGA internal structure diagram

4 System software design

4.1 FPGA software implementation

The design uses VIVADO integrated environment and Verilog HDL as the FPGA programming language. Verilog HDL has features that are independent of the specific hardware circuitry and platform-independent. It can model and describe digital systems from multiple levels, greatly simplifying hardware design tasks and improving design efficiency and reliability. The overall

design of the system uses a modular design approach. Starting from the system-level design, the system is divided into several basic units, and then each basic unit is divided into the basic units of the next level, and so on, until it can be directly implemented by the basic unit in the component library. The software development process of FPGA is shown in Figure 4.

Fig. 4. Software design flow chart

4.2 PID algorithm

PID (Proportional Integral Differential) algorithm has clear structure, convenient parameter adjustment and strong robustness. The PID algorithm is simple and efficient. Simulated PID algorithm expressions such as (1) [1]

$$u(t) = K_p [e(t) + \frac{1}{T_i} \int_0^t e(t) + T_d \frac{de(t)}{dt}] \quad (1)$$

Where K_p is the proportional gain, T_i is the integral time constant, and T_d is the differential time constant. By adjusting these three parameters, the system is stabilized.

In the digital control system, the discretization of (1) must be performed. A series of sampling points are used to represent the team's continuous time t discretization, and the integral is replaced by the sum, and the differential is used instead of the differential. The discrete digital PID control expression can be obtained as:

$$u(k) = K_p \left\{ e(k) + \frac{T}{T_i} \sum_{j=0}^k e(j) + \frac{T_d}{T} [e(k) - e(k-1)] \right\} \quad (2)$$

$$u(k) = K_p e(k) + K_I \sum_{j=0}^k e(j) + K_D [e(k) - e(k-1)] \quad (3)$$

Where $u(k)$ is the computer output value at the k th sampling time; $e(k)$ is the deviation value input at the k th sampling time; $K_I = K_p T / T_i$ is the integral coefficient, $K_D = K_p T_d / T$ is Differential coefficient. This design uses the output control to directly control the corresponding PWM duty cycle and adjust the indoor

temperature. When the set temperature value is stabilized, the PID control is stopped, and when the temperature changes, the PID control is automatically started. In the design, the PID parameter range is selected according to the empirical method, and the FPGA is used to continuously find the optimal parameters within the parameter range to ensure that each PID control is optimal control. Utilize the powerful data processing capability of FPGA, compare the difference between the deviation value and the PID output value under different parameters each time to ensure that the absolute value of each difference found is the optimal parameter. Figure 5 shows the flow chart of the PID algorithm data operation. Figure 6 shows the waveform of the Modelsim simulation of the PID algorithm.

Fig. 5. Data operation flow chart

Fig. 6. PID algorithm Modelsim simulation waveform

5 Conclusion

This paper introduces an indoor temperature control system based on FPGA as the main processing chip, which satisfies the requirements for intelligent temperature control in building energy saving. As a controller in intelligent building system, FPGA has the advantages of convenient programming and modification, high integration, small size and high reliability. Further research and experimentation is being carried out in conjunction with the actual situation. At the same time, there are still many places to upgrade. For example, voice control can be implemented, and the wristband can be connected to the smart wristband to automatically

control the temperature by measuring the body temperature. The combination of FPGA technology and other new technologies will promote the further development of intelligent building control systems and have a good development prospect.

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