A New Dynamic Voltage Restorer with Multi-level Open-end Winding Topology

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Abstract. In this paper, a variety of main circuit structures of DVR based on open-end winding are presented. Two inverters are connected in series to realize the multi-level structure and simplify the hardware cost. According to the mathematical model of open-end DVR, a three loop control strategy based on load voltage feedback is implemented to suppress the resonance of LCL filter. Aiming at the common mode voltage problem of open-end winding DVR, a common mode voltage suppression strategy based SVPWM is proposed to completely suppress the common mode voltage of high frequency and low frequency of the system. Finally, an open-end DVR experimental platform is built to verify the effectiveness of the control strategy and modulation strategy.

1 Introduction

Power quality problems widely exist in petrochemical industry, power system, metallurgy and steel, electrified railway, urban construction and other industries, mainly caused by various asynchronous motors, transformers, thyristor converters, frequency converters and other equipment. Dynamic voltage restorer (DVR) can realize the voltage stability of the sensitive load side, so it becomes an effective solution for voltage sag and flash. When the grid voltage suddenly changes, DVR injects the series compensation voltage with controllable amplitude and phase to the distribution line, so as to realize the constant load voltage[1,2].

DVR is connected to power grid and load in series by transformer. Several typical DVR topologies are proposed in literature [3-4]. The widely used three-phase three leg or three-phase four leg two level converter or the multi-level Clamped converter used in high-power occasions. In the last century, Isao Takahashi, a Japanese scholar, put forward the concept of open-end winding for the first time: the topology of opening the neutral point of the stator winding of the motor and supplying power from both ends of the winding by two-level converters [5,6], which can be equivalent to a NPC topology outputting three-level phase voltage. In DVR, the contacts on both sides of the primary side of the transformer are connected in series between the grid and the load, while the contacts on both sides of the secondary side can be connected in series to the converter, forming an open-end winding topology. Compared with the traditional three-level converter, it optimizes the hardware structure and omits the clamp diode. Through the series connection of the converter, it can improve the utilization ratio of DC voltage. The

open-end topology can also reduce the value of DC voltage under the condition of compensating the same network voltage amplitude, which is more conducive to the design of DC side energy storage unit or super capacitor.

There are many different forms of open-end winding series structure. Different topologies can be selected for DVR specific application scenarios. In this paper, the open-end winding DVR structure is taken as the research object. Firstly, the topological structures of different open-end winding structures are given, and the suitable application scenarios of each structure are defined. The three loops control strategy of load voltage, inductance current and compensation voltage is realized. Based on the two-level open-end winding structure, the modulation strategy of common mode voltage suppression is completed. Finally, the effectiveness of topology and control strategy is verified by experiments.

2 Open-end winding DVR topology

(a) Two level open-end winding of the common DC bus

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Fig. 1. DVR main circuit of open-end winding

Fig.1 shows several main circuit of open-end winding DVR topologies. Fig. 1 (a) (b) shows two level open-end winning of the common DC bus and two level open-end winning of the independent DC bus. In the low-voltage application scenario, using two-level series structure can not only ensure the effective compensation of load voltage, but also be equivalent to three-level structure to reduce the harmonic content of compensation voltage. The advantage of the common DC bus is to reduce a group of DC sources, and the

energy storage battery can be controlled centrally. However, the disadvantage of common DC is that it needs the common mode voltage suppression, which can reduce the utilization of DC voltage. Under the condition of compensating the same voltage, the common DC structure needs to raise the DC voltage.

Fig. 1 (c) (d) shows three level open-end winning of the independent DC bus and three level open-end winning of the common DC bus. In some medium voltage application scenarios, in order to achieve high power output and ensure the power quality of medium and high voltage load, it is necessary for DVR device to adopt multi-level series connection, and two groups of NPC three level series connection can ensure the voltage compensation within 10kV. Fig. 1 (d) shows hybrid multi-level open end winning of the independent DC bus. When the voltage level requirement is not high, the topology of two groups of series inverters can be flexibly changed, which can also achieve multi-level output. At the same time, when one end of the inverter stops working due to fault, it can still ensure the other end of the inverter works normally, and improve the reliability of DVR device.

3 Control strategy of open-end winding DVR

Taking the structure of two-level open winding DVR of common DC bus shown in Fig. 1 (a) as an example, the main circuit is composed of two groups of two-level converters in series. In order to reduce the hardware cost, two groups of converters share the same group of DC bus, which is then transmitted to the grid and load through LC filter and isolation transformer. Due to the common DC bus structure, the three-phase DVR can be controlled separately for each phase. The single-phase static ABC coordinate system is established as follows:

$$U_i = U_c + i_f r_f + L_f di_f / dt = U_{x1} - U_{x2} \quad (1)$$

$$i_f = i_c + ni_l \quad (2)$$

$$i_c = C_f dU_c / dt \quad (3)$$

$$U_{dvr} = n(U_c - n(r_f i_l + L_f di_l / dt)) \quad (4)$$

$$U_2 = U_1 + U_{dvr} \quad (5)$$

Where U_1 and U_2 are the voltage at both ends of the transformer. U_{dvr} is the voltage value injected to compensate the load voltage, and the load is composed of L_l and r_l . The DVR filter is L_f , r_f and C_f , and the leakage impedance of the transformer is L_t and r_t . The transformer transformation ratio is 1: n. I_f , I_c and I_l are respectively filter inductance current, capacitance current and load current. The output voltage of the converter is U_i , which is composed of the voltage U_{x1} and U_{x2} (x=A,B,C) of inverter 1 and inverter 2.

According to formula (1), the mathematical model of the system in three-phase static coordinate system can be expressed as follows:

$$\begin{cases} U_a = U_{Ca} + L_{fa} \frac{di_{fa}}{dt} + i_{fa} r_{fa} = S_{a1} U_{dc} - S_{a2} U_{dc} = U_{a1} - U_{a2} \\ U_b = U_{Cb} + L_{fb} \frac{di_{fb}}{dt} + i_{fb} r_{fb} = S_{b1} U_{dc} - S_{b2} U_{dc} = U_{b1} - U_{b2} \\ U_c = U_{Cc} + L_{fc} \frac{di_{fc}}{dt} + i_{fc} r_{fc} = S_{c1} U_{dc} - S_{c2} U_{dc} = U_{c1} - U_{c2} \end{cases} \quad (6)$$

$S_{ij}(i=a,b,c; j=1,2)$ is the switch function of the inverter phase arm. The upper arm on is 1 and the lower arm on is 0.

Convert (6) to synchronous rotation coordinate system as follows:

$$\begin{cases} U_d = U_{Cd} + \omega L_f i_{fd} + L_f \frac{di_{fd}}{dt} + i_{fd} r_s = U_{d1} - U_{d2} \\ U_q = U_{Cq} + \omega L_f i_{fq} + L_f \frac{di_{fq}}{dt} + i_{fq} r_s = U_{q1} - U_{q2} \end{cases} \quad (7)$$

Therefore, the equivalent circuit in two-phase coordinate system is shown in Fig. 2.

Fig.2. Equivalent circuit in two phase rotating coordinate frame

Based on the DVR topology shown in Fig. 1 (a), the control principle of the device is analyzed. The control of DVR mainly includes two parts, namely, obtaining the voltage reference value compensated by DVR itself and outputting the corresponding compensation voltage according to the reference value. The compensation performance of DVR is closely related to the control strategy it adopts. At present, the most important linear control is divided into feedforward control and feedback control. Feedforward control is prone to compensation error in practice, and voltage feedback control is often used for precise control demand, as shown in Fig. 3.

Fig. 3. Schematic diagram of DVR feedback control

$$G_B(s) = \frac{\omega_0 / Q}{(s^2 + \omega_0 s / Q + \omega_0^2)} \quad (8)$$

Fig. 3 adopts three loop control, and the outer loop is the load voltage loop to stabilize the load voltage. The middle loop is filter inductor current loop, and the inner loop is DVR compensation voltage loop. The three loop design avoids the phase error and amplitude error caused by the transformer. The inductor current introduced can also ensure the rapidity of current control.

k_v , k_c and k_i are the control parameters of outer loop, middle loop and inner loop respectively. In the inner loop design, inductor current feedforward is introduced, and inductor current is introduced into the compensation voltage loop through band-pass filter. The expression of band-pass filter is as shown in formula (8), and its conduction frequency is the resonance frequency of LCL filter. Its purpose is to introduce resonance component in the control link to realize the resonance suppression of LCL filter and ensure the load voltage compensation effect.

4 Common mode voltage suppression modulation strategy

For the DVR structure with open-end winding, the DC side can choose either the independent DC bus structure or the common DC bus structure. Because the independent DC bus structure needs to provide two groups of DC sources, which increases the hardware cost, the common DC bus structure is often used in practical application. However, the common DC bus structure has its own problems [5]. First, its DC voltage utilization ratio is slightly lower than that of the independent DC bus structure, and second, the common mode DC bus contains zero sequence path. Because of the existence of zero sequence path between two groups of inverters, three times of zero sequence current will appear in the filter inductance current, and the filter capacitance has very poor ability to suppress the three times of current, so it will appear in the transformer. The zero sequence current component makes the transformer appear bias phenomenon, which affects the quality of DVR compensation voltage. The source of zero sequence current is that the output voltage of two groups of inverters contains common mode voltage. To suppress the zero sequence current is to eliminate the common mode voltage of the inverter.

As can be seen from Fig. 1 (a), the common mode voltage of each inverters is:

$$\begin{cases} U_{cm1} = (U_{a1} + U_{b1} + U_{c1}) / 3 \\ U_{cm2} = (U_{a2} + U_{b2} + U_{c2}) / 3 \end{cases} \quad (9)$$

Considering the switch function, the common mode voltage of DVR system is as follows:

$$U_{cm} = U_{cm1} - U_{cm2} = [(S_{a1} + S_{b1} + S_{c1}) - (S_{a2} + S_{b2} + S_{c2})] U_{dc} / 6 \quad (10)$$

The common mode voltage of the converter can be eliminated by ensuring that formula (10) is zero at any time.

Fig. 4. Voltage space vectors of the individual inverter

Table 1. Space vectors without differential value of CM

Composite vector	Space vector combination	INV1 common mode voltage	INV2 common mode voltage	Common mode voltage
OS	13'	$U_{dc}/3$	$U_{dc}/3$	0
	64'	$2U_{dc}/3$	$2U_{dc}/3$	0
OH	15'	$U_{dc}/3$	$U_{dc}/3$	0
	24'	$2U_{dc}/3$	$2U_{dc}/3$	0
OJ	35'	$U_{dc}/3$	$U_{dc}/3$	0
	26'	$2U_{dc}/3$	$2U_{dc}/3$	0
OL	31'	$U_{dc}/3$	$U_{dc}/3$	0
	46'	$2U_{dc}/3$	$2U_{dc}/3$	0
ON	51'	$U_{dc}/3$	$U_{dc}/3$	0
	42'	$2U_{dc}/3$	$2U_{dc}/3$	0
OQ	53'	$U_{dc}/3$	$U_{dc}/3$	0
	62'	$2U_{dc}/3$	$2U_{dc}/3$	0
	11'33'55'	$U_{dc}/3$	$U_{dc}/3$	0
Zero vector	22'44'66'	$2U_{dc}/3$	$2U_{dc}/3$	0
	77'	U_{dc}	U_{dc}	0
	88'	0	0	0

Fig. 4 shows the space vector of two-level structure inverter 1 and inverter 2. Different space positions 1~6 and 1'~6' are generated by their respective switch functions, and then they are arranged and combined according to the space angle to get the series space vector diagram of two-level structure inverter, as shown in Fig. 5 (a). It contains 19 voltage space vectors, among which seven voltage vectors do not produce common mode voltage difference to the system, as shown in Table 1. The space positions of seven voltage vectors are H, J, L, N, Q, S, O, and the spatial distribution is shown in Fig. 5 (b). After superposition of seven voltage vectors, the common mode voltage difference of the

system is zero, so there is no common mode current caused by common mode voltage difference in the grid connected current, which affects the power quality.

(a) Space voltage vector distribution

(b) Composite space vector without common mode voltage difference.

Fig. 5. Voltage space vectors the dual two-level series inverters

Fig. 5 (b) shows the composite space vector without common mode voltage difference. There are two construction modes for each composite vector (except zero vector). When DVR considers the specific pulse occurrence of each inverter, it is necessary to make two adjacent vectors of each inverter act in the unit switch cycle, so as to ensure that each switch is only turned on and off once in the switch cycle. Taking sector 1 as an example, in Fig. 5 (b), the composite vector u_s is composed of two groups of vectors: OS and OH. According to the triangle sine theorem, the vector lengths of OS and OH are respectively:

$$\begin{cases} |U_{OS}| = |U_s| \sin(30^\circ - \theta) / \sin 120^\circ \\ |U_{OH}| = |U_s| \sin(30^\circ + \theta) / \sin 120^\circ \end{cases} \quad (11)$$

Where θ is the operation angle of the composite vector. Considering the pulse generation rule, the OS vector is composed of 13', and the oh vector is composed of 24'. Because $|U_1| = |U_3| = 1/\sqrt{3}|U_{OS}|$, $|U_2| = |U_4| = 1/\sqrt{3}|U_{OH}|$, then:

$$|U_1| = |U_{s1}| = |U_s| \sin(30^\circ - \theta) / \sqrt{3} \sin 120^\circ \quad (12)$$

Assign the composite vector U_{s1} and U_{s2} to the respective vectors of each inverter, as shown in Fig. 4, U_{s1} is composed of two groups of vectors 1 and 2, and θ_1 is the operation angle of U_{s1} . U_{s2} is composed of two groups of vectors 3' and 4', and θ_2 is the angle between U_{s2} reverse direction and α axis. At this time, the acting length of vectors 1 and 3' is:

$$\begin{cases} |U_1| = |U_{s1}| \sin(60^\circ - \theta_1) / \sin 120^\circ \\ |U_3| = |U_{s2}| \sin \theta_2 / \sin 120^\circ \end{cases} \quad (13)$$

The comparison formula (12) and (13) can be concluded as follows:

$$\begin{cases} |U_{s1}| = |U_{s2}| = 1/\sqrt{3} |U_s| \\ \theta_1 = \theta + 30^\circ, \theta_2 = 30^\circ - \theta \end{cases} \quad (14)$$

It can be seen that inverter 1 and inverter 2 only need to generate their own vectors according to formula (14) to realize the common mode voltage difference suppression without changing the traditional two-level SVPWM pulse generation, which simplifies the program design.

The maximum value of the composite vector phase voltage peak value is $2\sqrt{3} U_{dc}/3$ in Fig. 5 (a). After the common mode voltage difference suppression, the DC voltage utilization rate slightly decreases, and the maximum value of the phase voltage peak value is U_{dc} , as shown in Fig. 5 (b). However, compared with the maximum phase voltage peak $U_{dc}/\sqrt{3}$ of traditional NPC topology, the voltage utilization ratio is still increased by 24.4%.

5 Experiment

In order to verify the above theoretical analysis, an open-end winding three-phase DVR experimental platform is built. The topological structure is shown in Fig. 1 (a), the main circuit parameters are shown in Table 2, and the software is realized by DSP28335 control chip.

Table.2 Parameters of the DVR system

Parameter	Value	Parameter	Value
Grid voltage/V	380	Transformer Leakage inductor L_t /mH	0.3
Frequency/Hz	4800	Transformation ratio n	5
Filter inductor L_f /mH	1.5	Load inductor L_l /mH	1
Filter capacitor C_f /mF	0.1	Load resistor r_l/Ω	1

Fig. 6 is the experimental waveform of grid voltage drop. CH1 is A-phase filtering inductor current, and CH2 is A-phase load current. CH3 is A-phase grid voltage, and CH4 is A-phase load voltage. Adjust the grid voltage to make it drop to 300V, and set the load voltage to 400V. At this time, the load voltage follows the command to maintain the load voltage unchanged. Through the common mode voltage suppression strategy, the zero sequence voltage of the filter inductor current is

guaranteed. At the same time, the validity of DVR three loop control strategy is verified.

Fig.6. Experimental waveform of grid voltage drop

Fig.7. Experimental waveform of inverter output voltage

Fig. 7 shows the output line voltage and filter inductor current of the inverter. It can be seen that through the open-end winding structure in series, the line voltage of the inverter is guaranteed to be five-level. The harmonic content of the compensation voltage of the inverter is reduced under the same filtering conditions, and the load voltage power supply quality is further guaranteed.

6 Conclusion

In this paper, the main circuit topologies of DVR with various open-end winding series structures are proposed to further improve the diversity of DVR applications. According to the mathematical model of open-end winding DVR, it is clear that the composite vector is composed of two groups of inverters. The three loop control strategy of load voltage outer loop, inductance current middle loop and compensation voltage inner loop is proposed to effectively suppress the compensation resonance voltage caused by LCL filter. According to the open-end winding structure, the common mode voltage suppression modulation strategy is analyzed, which can completely suppress the common mode voltage of the system. At the same time, the correctness of the three loop control strategy and common mode voltage suppression modulation strategy of the open-end winding topology is verified by experiments.

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