Control Techniques for the Cascaded and Cross-switched Multilevel Inverter - A Comparison

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Abstract Nowadays, the multilevel inverter has gained huge attention and has become more popularized in high voltage and high-power applications with low harmonics. As the number of output voltage increases, the harmonic content of the output voltage waveform decreases. In this paper, a comparison of cascaded H-bridge and cross-switched multilevel inverters for 7, 9, 15, 21 levels will be carried out. The different control techniques that will be used for carrying out comparisons are space vector pulse width modulation (SPVPWM), sinusoidal pulse width modulation (SPWM), and third harmonic injection pulse width modulation (THI-PWM) respectively. Here, the seven-level inverter is discussed mainly and can be extended to any number of levels.

Keywords—Multilevel Inverter, Total Harmonic Distortion, Sinusoidal Pulse Width Modulation, Third Harmonic Injection Pulse Width Modulation, Cross-Connected, Total Standing Voltage

Nomenclature

Abbreviation	Explanation
V_{ref2}	Reference voltage vector of a two-level hexagon
V_{ref4}	Reference voltage vector of four-level hexagon
V_{ndc}	Number of DC voltage sources
V(t)	The output voltage of the multilevel inverter (MLI)
A	Real axis
N_d	Number of switches in the current path respectively.
B	Imaginary axis
a_0, a_n, b_n	These are the coefficients of the Fourier transform
Θ	Angle made by V_{ref} vector
Θ_2	Angle made by V_{ref2} vector
Θ_4	Angle made by V_{re4}f vector
V_{ma}	The modulation signal
f_m	Modulating wave's peak frequency
F	Fundamental output frequency of the inverter
f_{cr}	Carrier wave's peak frequency,
V_m	Reference signal peak amplitude
V_{cr}	Carrier signal peak amplitude respectively, ma is the amplitude modulation index
V_{ref}	Reference voltage vector

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1 Introduction

Multilevel inverters have become more focused and popularized in the past few decades. Multilevel Inverter is a power electronic device that can be used for high/medium voltage and power conditions with advantages of low harmonics, lower dv/dt stress on power electronic devices, lower device ratings, and reduced switching frequencies. In addition to the given advantages, some other advantages are low Total Harmonic Distortion (THD), efficiency, reliability, etc. Because of these advantages they are considered as proven technology and hence entered industry successfully. A three-level multilevel inverter was the first multilevel inverter that was introduced in 1975.

The different conventional topologies [1-7] of multilevel inverters are Neutral Point Clamped (NPC), Flying Capacitor (FC), and cascaded H-Bridge inverters (CHB). These regular geographies enjoy their benefits and weaknesses, however the fundamental downside of these three geographies is the requirement for high-power electronic parts, with an increment in the quantity of levels. This importantly builds the expense and intricacy of staggered inverters. In view of these disadvantages analysts have thought of new geographies of staggered inverters with less exchanging parts. Alongside presenting novel staggered inverter geographies, various strategies for control procedures for staggered inverters have likewise been presented. These control strategies can likewise be called adjustment methods which are characterized into two sorts. They are high recurrence and low-recurrence adjustment. Low-frequency modulation techniques cannot be applied for high power applications even though having better harmonic profiles. These are classified as space vector and selective harmonic elimination. High-frequency modulation can be

further divided into Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) techniques. Because of all these factors, this paper proposes a comparison of the seven-level cascaded and cross-bridge multilevel inverter using different control techniques which are Sinusoidal Pulse Width Modulation [2,5,6,16,17], Space Vector Pulse Width Modulation [1,3], and Third Harmonic Injection Pulse Width Modulation respectively [4].

2 Cascaded H-Bridge Topology

Fig.1 shows a conventional stage seven-level customary cascade H-bridge geography [11,12,13]. The seven-level cascade H-bridge staggered inverter comprises of three series-associated single-stage H-spans per stage to which a secluded DC source is available for every H-connect. The fundamental downside of cascade H-connect is the requirement for disconnected force hotspots for each level and stage. The secluded design of indistinguishable H-bridge is a reassuring element. As every H-connect is taken care of by a similar worth of Dc voltage, it is known as a balanced fell H-bridge staggered inverter. Every H-bridge can produce three degrees of yield voltage, which are $+V_{dc}$, 0, $-V_{dc}$. The exchanging design is displayed in Table 1 and the yield voltage of the seven-level inverter can be found in Fig. 2. The proposed geography is customary and can be stretched out to any staggered inverter by utilizing the accompanying formulae.

1. The number of levels in line-to-line voltage waveform is k=2N-1
2. Per phase number of capacitors or isolated supplies are N_{cap}=(N-1)/2

Advantages of cascaded H-bridge are:

1. The number of DC sources required is half the number of output voltage levels.
2. The manufacturing process is quicker and cheaper.

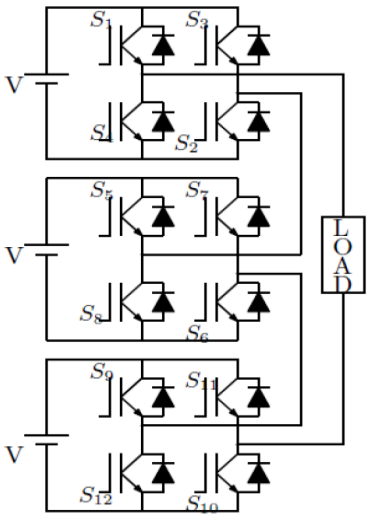


Fig. 1. Conventional cascaded 7 level inverter

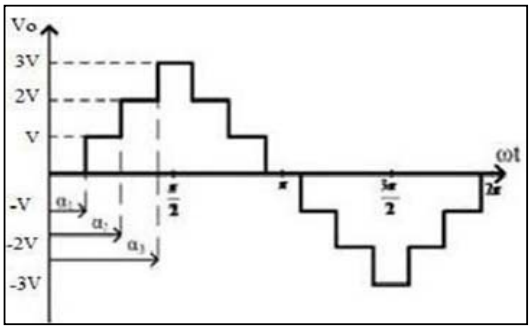


Fig. 2. The output voltage waveform of seven-level inverter [5]

Table 1. Switching sequence of seven-level inverter

V_0	+V	+2V	+3V	0	-V	-2V	-3V
S_1	1	1	1	0	0	0	0
S_2	1	1	1	1	0	0	0
S_3	0	0	0	0	1	1	1
S_4	0	0	0	1	1	1	1
S_5	0	1	1	0	0	0	0
S_6	1	1	1	1	1	0	0
S_7	0	0	0	0	0	1	1
S_8	1	0	0	1	1	1	1
S_9	0	0	1	0	0	0	0
S_{10}	1	1	1	1	1	1	0
S_{11}	0	0	0	0	0	0	1
S_{12}	1	1	0	1	1	0	1

2.1 Control of Cascaded H-Bridge Inverter using Sinusoidal Pulse Width Modulation (SPWM)

The sinusoidal pulse width modulation technique [8,9,14] is a simple modulation technique used for harmonic reduction in inverters. In this technique, the pulse magnitude will be constant, and the pulse width is changed. Here, a reference wave is compared with a carrier wave and generates gate pulses. For this, a pure sine wave (reference) is compared with a triangular wave (carrier). The fundamental frequency is taken for the sine wave, and more than the fundamental frequency can be taken for the carrier wave. If the number of levels is m, then (m-1) triangular carrier waves are required. So, a seven-level inverter requires six carrier waves.

Two important parameters are defined in modulation techniques:

1. The frequency ratio $m_f = \frac{f_{cr}}{f_m}$
2. Amplitude modulation index $m_a = \frac{V_m}{V_{cr}(m-1)}$

The fundamental frequency component in the inverter output voltage can be controlled by the amplitude modulation index. Where f_m is the modulating wave's peak frequency, f_{cr} is the carrier wave's peak frequency, V_m is the reference signal peak amplitude and V_{cr} is carrier signal peak amplitude respectively. The amplitude modulation index m_a is usually adjusted by varying V_m

and keeping V_{cr} fixed. The frequency of the reference signal determines inverter output frequency and its peak amplitude controls modulation index and in turn RMS output voltage. The SPWM scheme used here is level shifted in phase disposition (IPD) as it has a lower harmonic profile compared to other conventional techniques. The gating pulses for the switches S_1, S_2 are provided by carrier waves V_{cr1} and V_{cr1-}, the innermost carrier pair $V_{cr3}$and V_{cr3-} generate pulses for switches S_9&S_{11}. The remaining carrier waves V_{cr2} and V_{cr2-} generate gating pulses for S_5 & S_7. Fig.3 shows level-shifted PWM for a seven-level cascaded H-bridge inverter. The switches S_1, S_5, S_9 are turned on for the carrier waves above zero reference when modulating signal V_{mA} is higher than carrier waves, and the switches S_3, S_7 & S_{11} are turned on for the carrier waves below the zero reference when modulating wave V_{mA} is lower than carrier waves.

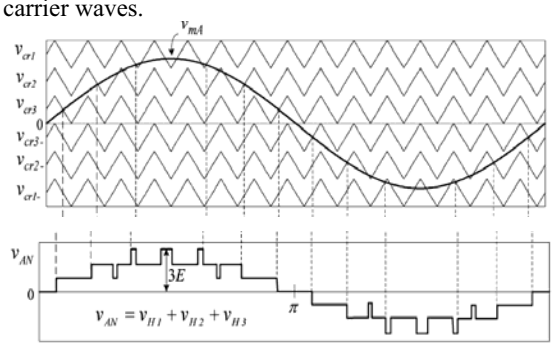


Fig. 3. Level-shifted PWM for a seven-level CHB inverter (m_f = 15, m_a= 0.8, f_m=60 Hz, and f_{cr} = 900 Hz).

The results can be seen in Table 5, and the fundamental output voltage can be seen in Fig. 8(b) & 9(b) for various modulation indices.

2.2 Control of Cascaded H-Bridge using Space Vector Pulse Width Modulation (SVPWM)

The conventional 7-level space vector pulse width modulation (SVPWM) has a total of 216 two-level hexagons. As high quantities of triangles are included, the execution of this technique is exceptionally intricate in seven-level inverter. Thus, an improved on SVPWM method is utilized in this paper which is known as a further worked on space vector adjustment strategy (FSSVM) [3,11,12,13] which is simpler contrasted with a regular procedure. By utilizing this method, the intricacy and exertion of the seven-level SVPWM become equivalent to the five-level SVPWM procedure. Here at first seven-level space vector chart is settled into six four-level hexagons and afterward every four-level hexagon into seven two-level hexagons. In this manner the all-out two-level hexagons to be considered here are just 42. The space vectors incorporate fixed vectors and there is one turning vector V_{ref} which pivots at a speed of ω = 2πf in space, where f is the central yield recurrence of the inverter. V_{ref} is known as a kind of perspective vector. For the ordinary activity of the inverter, the extent of V_{ref} relies on the regulation file, which goes from zero to one. By using the stationary vectors available, the V_{ref} vector is synthesized as closely as possible, which is the basic principle of space vector pulse width modulation. By identifying the triangle in which the tip of V_{ref} lies we can synthesize V_{ref} conventionally. "Nearest Three Vectors" (NTVs) are formed by the vertices of this triangle for V_{ref} and it is then synthesized by using these three vectors. After every sampling period (t_s) this operation is repeated.

In the FSSVM technique, the space vector diagram is initially resolved into six four-level hexagons. Along 0°-axis the center of the first four-level hexagon lies, and each subsequent hexagon center is shifted by 60°. There is overlapping between adjacent hexagons as shown in Fig. 4. Depending upon the angle 'Θ'of the original reference vector V_{ref} of conventional space vector diagram, the appropriate four-level hexagons are selected which is shown in Table 2.

After the selection of a four-level hexagon, a new reference vector V_{ref4} is generated at the center of the four-level hexagon. The tip of V_{ref4} coincides with the tip of Vref and both can b related as follows:

$$V_{4\alpha} = V_{7\alpha} - 2E \quad (1)$$

$$V_{4\beta} = V_{7\beta} \quad (2)$$

Where α is the real axis and β is the imaginary axis and $V_{7\alpha}, V_{7\beta}, V_{4\alpha}, V_{4\beta}$ are components of V_{ref} and V_{ref4} respectively. Table 3 shows the computation of V_{ref4} for all the six four-level hexagons. The range of modulation index for the vector V_{ref4} is from zero to unity and an angle Θ_4 ranging from zero to 2π.

The following stage is to determine these four-level hexagons into 42 two-level hexagons. These two-level hexagons are partitioned into two kinds. They are internal hexagon(IH) and outer hexagon(OH). Here every four-level hexagon is settled into seven two-level hexagons. Contingent upon the point and extent of the V_{ref4} vector, the determination of two-level hexagons is done and is displayed in Table 4. The span of encompassing circle is 2E/3 for a two-level hexagon. Subsequently if the extent of V_{ref4} is not exactly or equivalent to 2E/3 then the internal hexagon is chosen and assuming the size of V_{ref4} is more noteworthy than 2E/3 one of the external hexagons is chosen which can be displayed in Table 4. The vector V_{ref4} beginning is equivalent to the two-level reference vector beginning when the inward hexagon is chosen. Nonetheless, another reference vector V_{ref2} should be created when the external two-level hexagon is chosen.

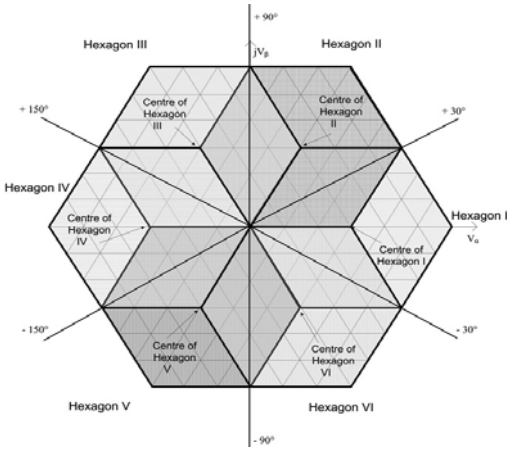


Fig. 4. Division of seven-level SVD into six four-level hexagons [3]

The modulation index (m_a) is defined as the maximum value m_a=1, to the maximum radius of the circle that can be inserted in the space vector diagram, this can be seen in Fig. 6. When the dark portion of the space vector diagram isn't included then six outer hexagons(OH) are considered for m_a=1 and all the 42 two-level hexagons are included in the space vector diagram.

Table 2. Selection of four-level hexagon

Hexagon number	Range of Θ
I	-30^0 to $+30^0$
II	$+30^0$ to $+90^0$
III	$+90^0$ to $+150^0$
IV	$+150^0$ to -150^0
V	-150^0 to -90^0
VI	-90^0 to -30^0

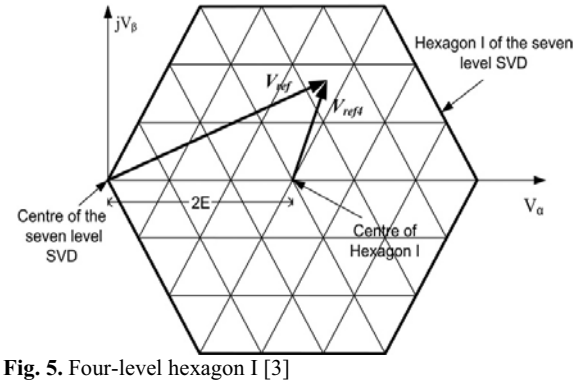


Fig. 5. Four-level hexagon I [3]

Table 3. Computation of V_{ref4} from V_{ref}

Hexagon	$V_{4\alpha}$	$V_{4\beta}$
I	$V_{7\alpha} - 2E$	$V_{7\beta}$
II	$V_{7\alpha} - 2E\cos\frac{\pi}{3}$	$V_{7\beta} - 2E\sin\frac{\pi}{3}$
III	$V_{7\alpha} - 2E\cos\frac{2\pi}{3}$	$V_{7\beta} - 2E\sin\frac{2\pi}{3}$
IV	$V_{7\alpha} + 2E$	$V_{7\beta}$
V	$V_{7\alpha} - 2E\cos\frac{4\pi}{3}$	$V_{7\beta} - 2E\sin\frac{4\pi}{3}$
VI	$V_{7\alpha} - 2E\cos\frac{5\pi}{3}$	$V_{7\beta} - 2E\sin\frac{5\pi}{3}$

Table 4 describes the selection of particular two-level hexagons which depend on the magnitude and angle of the reference vector V_{ref4}. Where V_{ref4} is the reference voltage of a four-level hexagon. After the selection of a two-level hexagon, calculation of dwell time and selection of switching sequence is carried out to give appropriate gate pulses to the proposed inverter by using the basic principle of two-level SVPWM respectively. The vectors V_{ref2} and V_{ref4} are related as follows:

$$V_{2\alpha} = V_{4\alpha} - \frac{4E}{3} \quad (3)$$

$$V_{2\beta} = V_{4\beta} \quad (4)$$

In this technique, the complexity is reduced but as a result, total harmonic distortion (THD) is increased for the modulation index $m_{a4} > 0.774$ of a four-level space vector diagram. For $m_{a4} < 0.774$ no part of the space vector diagram is left untouched and if V_{ref4} lies in the dark unattended part then one of the outer hexagons is selected depending on the angle Θ_4 of V_{ref4}. Thus a new reference vector V_{ref2} is generated with its origin at the center of the two-level hexagon and thus depending on the angle of V_{ref2}, the appropriate sector will be selected and the SVPWM technique is carried out. The results can be seen in Table 5, and the fundamental output voltage can be seen in Fig. 8(a) & 9(a) for various modulation indices.

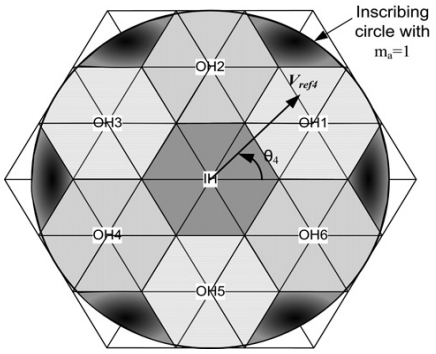


Fig. 6. Four-level SVD with inscribing circle for m_a = 1[3]

Table 4. Selection of a two-level hexagon in FSSVM technique

Two-level hexagon	Magnitude of V_{ref4}	Angle Θ_4 of V_{ref4}
IH	$\leq 2E/3$	-
OH1	$\geq 2E/3$	0^0 to 60^0
OH2		60^0 to 120^0
OH3		120^0 to 180^0
OH4		-180^0 to -120^0
OH5		-120^0 to -60^0
OH6		-60^0 to -0^0

2.3 Control of Cascaded H-Bridge using Third-Harmonic Injection Pulse Width Modulation (THIPWM)

The sinusoidal pulse width balance procedure is not difficult to execute just as to comprehend. However, the fundamental disadvantage of this strategy is, it can't use the whole accessible DC transport supply voltage and subsequently this technique approaches less of the greatest attainable yield voltage. Along these lines, a third consonant infusion beat width adjustment procedure [4,11,12,13] is acquainted with defeat this issue. In this technique, by adding a third consonant sign in a low-recurrence sinusoidal reference signal we can accomplish the abundancy expansion in yield voltage waveform. The expansion of third music implies that in one pattern of a sinusoidal wave, three patterns of music will finish. The consequence of the expansion of the third symphonious and basic consonant is less in sufficiency than the key consonant. This method helps the inverter in its performance enhancement. Fig. 8 shows the fundamental voltage (V_m), third harmonic content ($\frac{V_m}{n}$), and the modulation signal V_{ma}. In this paper, a basic third harmonic injection pulse width modulation is carried out

for a seven-level inverter and The results can be seen in Table 5, and the fundamental output voltage can be seen in Fig. 8(c)&9(c) for various modulation indices.

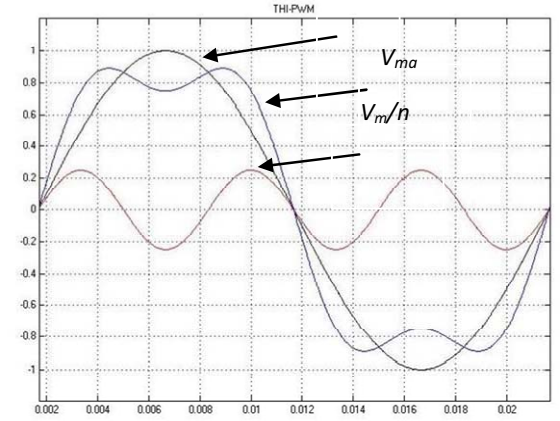


Fig. 7(a)

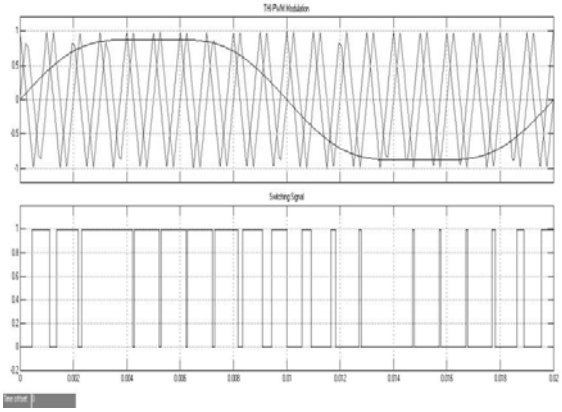


Fig. 7(b)

Fig.7. Third Harmonic Injection pulse width modulation [4]
a) generating third harmonic injected modulating signal,
b) multicarrier and modulating signals utilized in generating switching signals

2.4 Comparison of Control Techniques for Cascaded H-Bridge

The advantages of the space vector pulse width modulation technique over sinusoidal pulse width modulation are that it provides more fundamental output voltage also is flexible for the design of switching patterns and is better suited for digital implementation. Thus, space vector pulse width modulation technique is considered a popular choice for industrial applications. The fundamental component of output voltage and Total Harmonic Distortion (THD) obtained in the space vector pulse width modulation scheme is greater than the sinusoidal pulse width modulation scheme. It is better to use the third harmonic injection pulse width modulation scheme if the sole purpose is the total harmonic distortion reduction. As no FSSVPWM or SPWM can compare with THI-PWM as far as total harmonic distortion is dealt with. For modulation index m_a<0.2 or m_a=0.2, the FSSVPWM shows remarkable improvement over SPWM and THI-PWM schemes. This is useful in cases where the inverter is sometimes required to function at low modulation indices. The results can be seen in Table 3, and fundamental output voltages for the three discussed control techniques can be seen in Fig. 8&9 for various modulation indices.

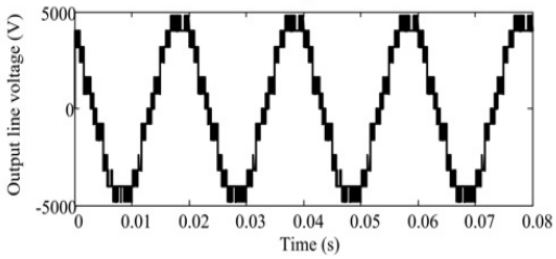


Fig. 8(a)

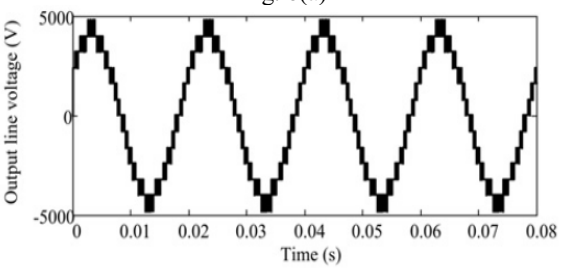


Fig. 8(b)

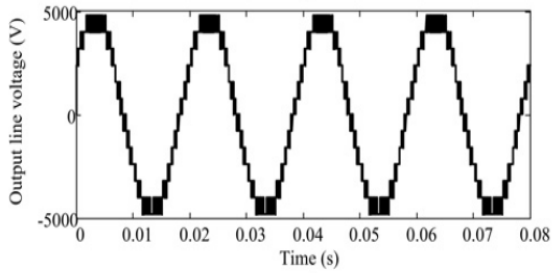


Fig. 8(c)

Fig. 8. Output line voltage waveforms at ma = 1[3] for
a FSSVPWM
b SPWM and
c THI technique

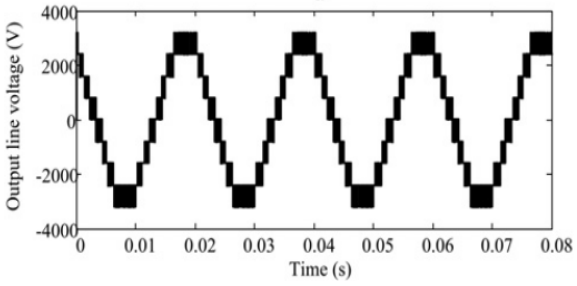


Fig. 9(a)

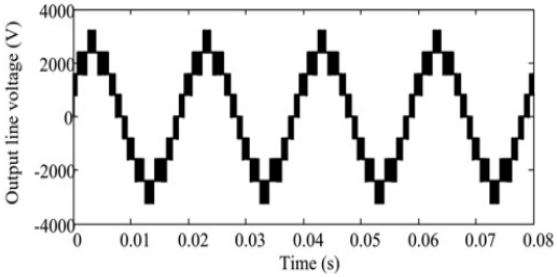


Fig. 9(b)

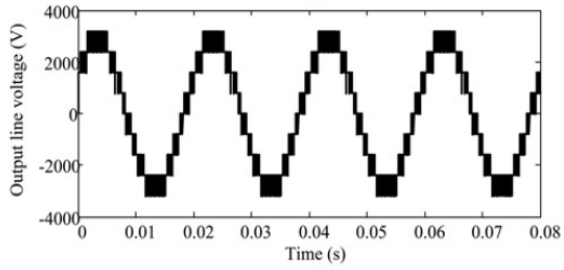


Fig. 9 (c)

Fig. 9. Output line voltage waveforms at m_a = 0.6 [3] for
a FSSVM
b SPWM and
c THI technique

Table 5. THD and peak value of the fundamental component (V_{1m}) of output line voltage

Modulation Technique		FSSVPWM	SPWM	THI-PWM
m_a = 1.0	THD,% V_{1m}, V	16.36 4631	10.62 4158	9.16 4801
m_a = 0.8	THD,% V_{1m}, V	15.77 3764	13.33 3325	12.32 3841
m_a = 0.6	THD,% V_{1m}, V	19.81 2892	17.26 2492	16.66 2879
m_a = 0.4	THD,% V_{1m}, V	30.29 2013	25.55 1662	24.37 1918
m_a = 0.2	THD,% V_{1m}, V	39.4 1405	49.13 831.9	44.61 961.3
m_a = 0.1	THD,% V_{1m}, V	36.53 1452	120.39 415.6	105.99 478.6

3 Cross-Bridge Multilevel Inverter Topology

By utilizing the ideas of ordinary cascade H-bridge and the multi-string staggered inverter, the seven-level cross-exchanged staggered inverter geography [2,6,16,17] is planned. This geography comprises of six force semiconductor switches and two DC voltage sources. The switches are addressed as S_1, S_2, S_3, S_4, S_5, and S_6, while the DC sources are addressed as E_1 and E_2. From Fig. 10 two switches (S_5 & S_6) are available in the center and as they are sharing the voltage from both DC sources, they have the most noteworthy voltage appraisals. A proportion of 2:1 is kept up with by DC sources which infer unbalanced setup. From Fig. 10 the switches S_1 & S_2 which are near to the source E_1 will have a voltage rating of $2V_{dc}$ and they contribute to generate voltage levels $-V_{dc}$, 0, $2V_{dc}$. Similarly, the switches S_3&S_4 which are near to source 2 will have a voltage rating of V_{dc} and they contribute to generate three voltage levels $-V_{dc}$, 0, $+V_{dc}$. The middle switches S_5 & S_6 will produce $+3V_{dc}$ & $-3V_{dc}$ respectively.

Total seven output voltage levels $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, $2V_{dc}$, $3V_{dc}$ are generated. Also, the odd-numbered switches operate in a complementary manner to the even-numbered switches. Table 6 shows the switching sequences of the proposed topology.

By extending this to more levels the voltage capacity of the inverter can be increased. So, this proposed topology can be extended to N-levels by using the below formulae:

$$N_{Switch} = N_{Level} - 1 \quad (5)$$

$$N_{DC\_supplies} = N_{Switch}/3 \quad (6)$$

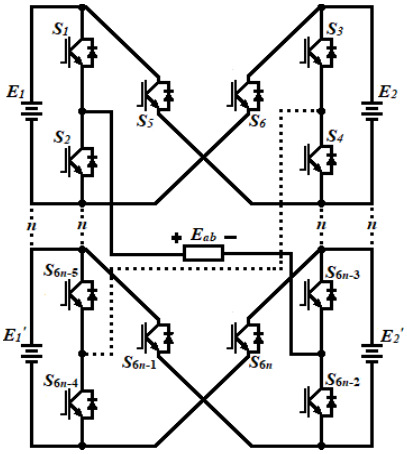


Fig. 10. Single-phase N-level cross switch multilevel inverter [1]

Table 6. Switching sequences of 7-level cross switch multilevel inverter

Switching States			DC Supply Voltages		Total Voltage
S_1	S_5	S_3	E_1	E_2	E_{ab}
1	0	0	$2V_{dc}$	V_{dc}	$3V_{dc}$
1	1	0	$2V_{dc}$	0	$2V_{dc}$
0	0	0	0	V_{dc}	V_{dc}
0	1	0	0	0	0
1	0	1	0	0	0
1	1	1	$-2V_{dc}$	V_{dc}	$-V_{dc}$
0	0	1	$-2V_{dc}$	0	$-2V_{dc}$
0	1	1	$-2V_{dc}$	$-V_{dc}$	$-3V_{dc}$

3.1 Control of Cross-Bridge using Sinusoidal Pulse Width Modulation (SPWM)

The sinusoidal pulse width modulation technique [2,6,16,17] is used to generate the gate pulses and seven-level output of the cross switch multilevel inverter. The carrier wave modulation technique is one of the types of SPWM, which is again divided into two types i.e., phase-shifted carrier modulation (PSCM) and level shifted carrier modulation (LSCM). In this paper, we are considering the LSCM technique as it has advantages like low harmonics and more flexibility to operate inverter at different switching frequencies compared to PSCM. Here, phase opposition disposition (POD) is used to generate the six carrier waves. Where carrier waves above the zero reference are in phase among each other whereas out of phase to those below the zero references. Six carrier waves V_{cr2}, V_{cr3}, V_{-cr1}, V_{-cr2}, and V_{-cr3} as shown in Fig. 10 are required for cross switch topology as it generates seven output voltage levels. An amplitude of A_{cr} and frequency of f_{cr} are possessed by each carrier wave. Whereas the sinusoidal reference voltage V_{ab_ref} is having a frequency of 50Hz and amplitude of 1 to

generate the signal pulse. Thus, the frequency modulation and amplitude modulation indices are given below:

$$m_f = \frac{f_{cr}}{f} \quad (7)$$

$$m_a = \frac{A_m}{A_{cr} \times \frac{N_{level}-1}{2}} \quad (8)$$

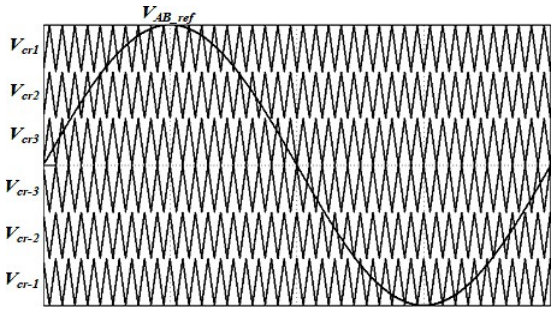


Fig.11. SPWM using carrier waves following level-shifted POD [2].

The block diagram in Fig. 12 gives the control and implementation of SPWM. In this technique, carrier waves are compared with the sinusoidal reference wave. If the modulating wave (reference) is greater than the positive carrier waves, then the output of '1' else '0' will be obtained. On adding the pulses (*Pl*) obtained from the above comparisons we will get the switching states (SW) as below:

$$SW = (Pl_1 + Pl_2 + Pl_3) + (Pl_{-1} + Pl_{-2} + Pl_{-3}) \quad (9)$$

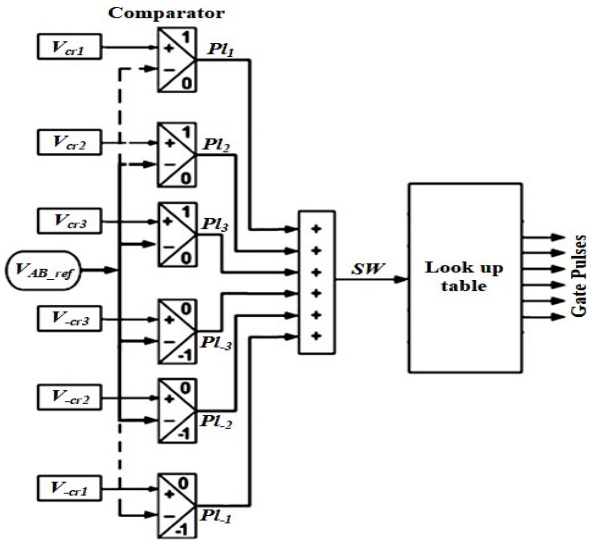
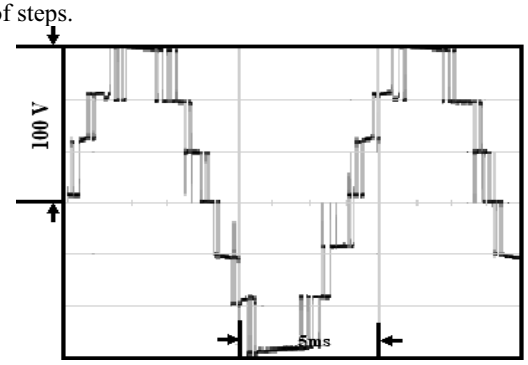
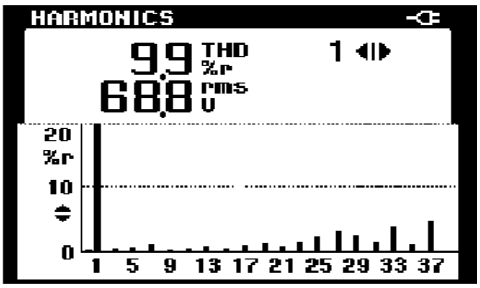


Fig. 12. The control diagram of the SPWM technique for cross-switched MLI [2].

On comparing switching states with the lookup table, we will get six gate pulses and these pulses are used by the multilevel inverter to generate output seven-level voltage. The harmonic distortions in Fig. 13 are obtained by taking E_1=66.67V_{dc} and E_2=33.33V_{dc} and considering R-L load (R=237Ω, L=0.53H) the simulation results are obtained. From the below results we can say that as the modulation ratio is decreased, the output and RMS voltages are reduced. As a result, fewer numbered output steps are obtained, and total harmonic distortion (THD) got increased as the inverter is generating a lower number of steps.



(a)



(b)

Fig. 13. Experimental results at *m* = 1for SPWM [2]:
(a) 7-level output voltage
(b) THD and RMS voltage.

3.2 Control of Cross-Bridge using Space Vector Pulse Width Modulation (SVPWM)

In the proposed multilevel inverter topology we use one-dimensional SVPWM control [1,6,16,17] over conventional control. As the conventional SVPWM techniques involve complex mathematical calculations and also due to its large switching states. E_1 and E_2 of the given cross switched topologies give -2V_{dc}, 0, 2V_{dc}, and –V_{dc}, 0, V_{dc} respectively and whose voltage levels are represented as 0,1,2 in this control region. In Fig. 14 the state XY corresponds to the cross switch inverter having states X & Y represents E_1 & E_2 supplies respectively.

Fig. 15 shows the stream chart which utilizes the necessary numerical computations in one-dimensional control to acquire exchanging arrangements and exchanging times. Here the sinusoidal wave with recurrence 50Hz and modulation index=1 is chosen as reference voltage V_{ab_ref}. The reference voltage V_{ab_ref} is standardized with DC voltage step V_{dc} to acquire the positive reference voltage 'a'. The contrast between two continuous voltage levels is called step and it is consistently steady which can be found in Fig. 14. The capacity floor ‘a’ rounds of the components of 'a' to its closest number which is not exactly or equivalent to 'a' to decide the 'simulated intelligence' factor. Hence, acquired whole number variables are utilized to decide exchanging states and times. Always the switching sequences formed

by the switching states $S_1=a_i$, $S_2=a_i+1$ with switching times $t_1=1-r$ & $t_2=r$ respectively. Thus, the final switching sequence 'S_p' is determined by comparing S_p repeatedly with the lookup table we will obtain seven gate pulses and then these are used for switches of multilevel inverter.

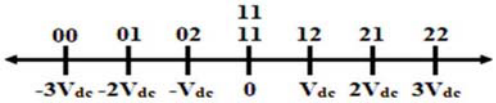


Fig. 14. One dimensional control region for seven-level cross-switched MLI [1].

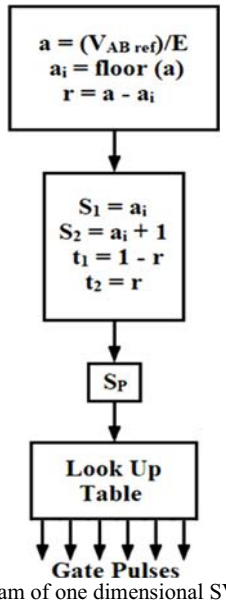


Fig. 15. Flow diagram of one dimensional SVM control of single-phase [1]

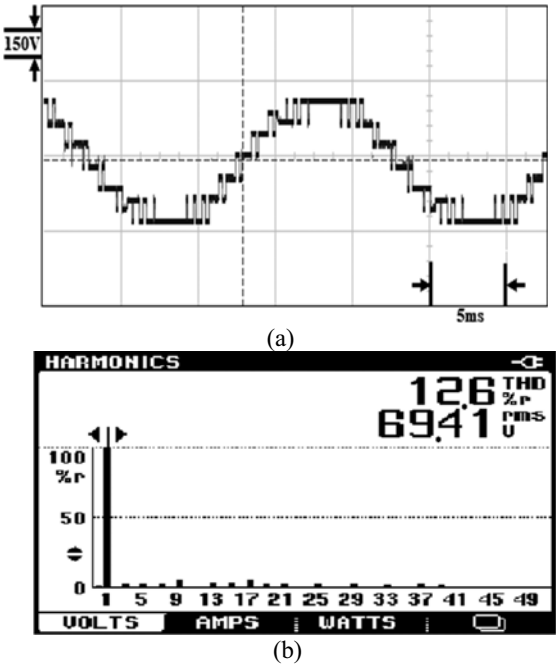


Fig.16. Experimental results of SVPWM for the cross-switched MLI [1].
(a) Seven steps output voltage at m = 1.
(b) THD and RMS voltage at m = 1.

The harmonic distortions in the below Fig. 16 are obtained by taking $E_1=66.67V_{dc}$ and $E_2=33.33V_{dc}$ and considering R-L load (R=237Ω, L=0.53H) the simulation results are obtained. From the below results we can say that as the modulation ratio is decreased, the output and RMS voltages are reduced. As a result, fewer numbered output steps are obtained, and total harmonic distortion (THD) got increased as the inverter is generating a lower number of steps.

Table 7. Comparison of SVPWM and SPWM control techniques for seven-level cross-bridge inverter

Modulation Technique		Space vector pulse width modulation (SVPWM)	Sinusoidal pulse width modulation (SPWM)
m_a = 1.0	THD, % V_{rms}	12.6 69.41	9.9 68.8
m_a = 0.8	THD, % V_{rms}	19.4 45.17	13.6 54.7

4 Comparison of a cross switch and cascaded h-bridge multilevel inverters

Here the acquired outcomes from the over seven-level cross-connect geography are contrasted and symmetric cascade H-connect geography. Five elements are thought about for the correlation of both the geographies. They are the quantity of switches, power misfortune, Total Standing Voltage(TSV) of influence semiconductor gadgets, at any moment the quantity of gadgets in the current way, and all total harmonic distortion(THD).

Table 8 shows the examination of the quantity of switches for fell H-extension and cross-connect inverters for 7,9,15 and 21 levels individually. From Table 8, we can infer that cross switch geography utilizes a lower number of switches contrasted with fell H-connect geography. As the quantity of switches is diminished importantly driver circuits required and intricacy can likewise be decreased in cross switch staggered inverter contrasted with fell H-connect.

Fig.17 shows that the total standing voltage(TSV) of both cascaded and cross-bridge inverters are the same for seven-level or any other greater levels of multilevel inverters. Mathematically we can see from the below formulae:

$$(TSV_{cross}/V_{dc}) = 2(N_l-1) \text{ and} \quad (10)$$
$$(TSV_{cascaded}/V_{dc}) = (TSV_{cross}/V_{dc}) \quad (11)$$

Thus the Fig.18 shows the cross-switch topology has fewer series devices as compared to cascaded H-bridge topology in the current path, which implies that the voltage drops, and conduction losses of a cross switch are less compared to cascade. The number of switches in the current path of seven-level cross-switch topology is 4, whereas in cascaded H-bridge is 6. For N-levels (N_l) we can find the number of switches in the current path (N_d) by using the below formulae:

$$N_d, cross = \frac{N_l+1}{2} \quad (12)$$

$$N_d, CHB = N_l - 1 \quad (13)$$

Another factor of comparison is power losses. From Fig. 19 the cross-bridge topology has lower losses than cascaded H-bridge topology. This is because cross-bridge topology is having lower devices in the current path at any instant of time.

Table 8. Comparison of the number of switches for cascaded and cross-bridge inverters.

Cascaded H-bridge inverter level	Number of switches	Diodes	DC sources	Total compo nents
7	12	12	3	27
9	16	16	4	36
15	28	28	7	63
21	40	40	10	90
Cross bridge inverter level	**Number of switches**	**Diodes**	**DC sources**	**Total compo nents**
7	6	6	2	14
9	8	8	3	19
15	14	14	5	33
21	20	20	7	47

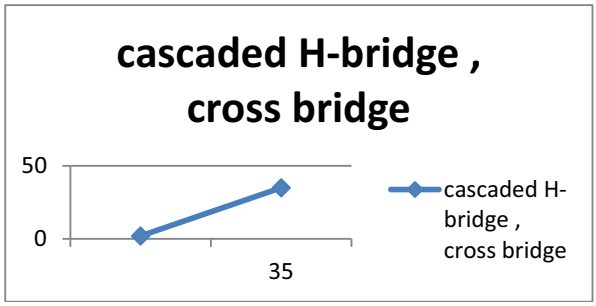


Fig. 17. The total standing voltage of switches against the number of voltage levels (N_l) in cascaded H-bridge and cross-bridge topologies

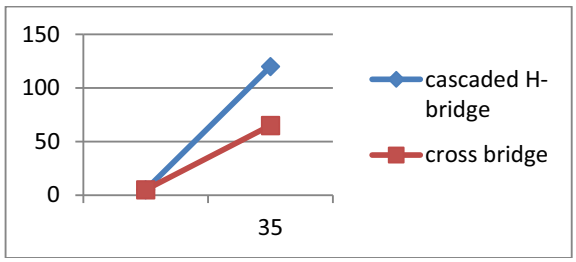


Fig. 18. Number of switches in the current path (N_d) against the number of voltage levels (N_l) in cascaded H-bridge and cross-bridge topologies

The total harmonic distortion (THD) factor can likewise be thought of while contrasting both seven-level fell H-extension and cross-connect. From Table 5 we can infer that the third harmonic distortion gives low harmonic for modulation index more noteworthy than 0.2 and the FSSVPWM method gives lower music for regulation list lesser than 0.2. Essentially, from Table 7, we can presume that the SPWM procedure gives lower music contrasted with the SVPWM strategy for the proposed seven-level cross switch geography. These outcomes apply to any more significant level inverters individually. On the off chance that we look at traditional geographies, we can presume that cross-connect geography will have lower symphonious mutilations contrasted with fell H-connect. The upsides of cascade H-bridge geography over cross-connect are its accessibility of adaptation to internal failure i.e., if one of the H-spans is broken even, it tends to be skirted, and other H-spans supply the load.

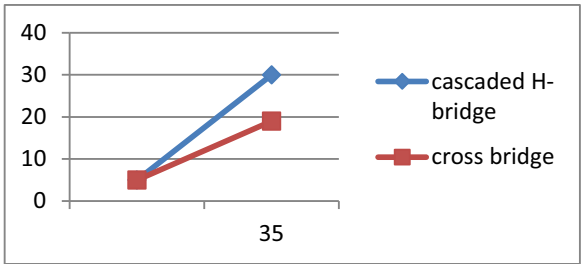


Fig. 19. Switching losses (P_{loss}) against the number of voltage levels (N_l)in cascaded H-bridge and cross-bridge topologies

5 Conclusion

In this paper different control techniques, which are sinusoidal pulse width modulation, space vector pulse width modulation, third harmonic injection pulse width modulation are discussed and compared. From these control techniques we can conclude that for low total harmonic distortions, third harmonic injection pulse width modulation is considered over the other two. For modulation indices less than or equal to 0.2 and for better fundamental voltage we use space vector pulse width modulation techniques respectively for seven-level cascaded H-bridge. Additionally, we can presume that the SPWM method gives lower music contrasted with the SVPWM strategy for the proposed seven-level cross switch geography. Likewise in this paper, we analyzed cascade H-bridge and cross-connect topologies for various levels for the variables: number of switches, absolute standing voltage, and number of switches in the current way at any moment, power misfortunes, and complete consonant twists. It tends to be reasoned that cross-switch topology performs better compared to cascade H-bridge topology particularly when there is a restriction in the quantity of switches. The cross-switch geography doesn't utilize high voltage switches and consequently it tends to be utilized for high voltage applications. As there are fewer switches in the current path in cross switch topology, the switching losses are also low compared to the cascaded H-bridge topology.

6 Acknowledgement

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