Bulk-driven current conveyor optimization using simulation-based method

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Abstract. This paper presents the optimization of a novel low-voltage (LV) and low-power (LP) bulk driven current conveyor (CCII). For the bulk-driven circuits, the transistors are biased at the subthreshold regime for LV and LP operation. In contrast, the input transistors of the differential stage are controlled from the bulk terminals to achieve a rail-to-rail input voltage range. A simulation-based technique is adapted for the optimal design of LV-LP bulk driven CCII, using the single-objective particle swarm optimization (PSO) algorithm. It is designed using CMOS 0.18 µm technology to operate at a voltage of 0.3 V and have a power consumption of 37 nW. Optimization results and also process/temperature corner results confirm the correct operation of the designed circuit.

1 Introduction

Low voltage and low power CMOS integrated circuits (ICs) have a wide range of applications in implantable and portable electronic systems [1, 2]. In recent decades, various IC methods were proposed and developed to address the design constraints related to LV operation [3]. In addition, the application of sub-threshold voltage biased bulk-driven (BD) transistors has attracted considerable attention allowing the design of circuits powered by sub-0.5V voltage and rail-to-rail signal swing [4, 5].

Current conveyors are flexible active building blocks that can be used for both current-mode and voltage-mode analog IC applications [6]. The CCII has the advantage of being easily realized in bipolar and CMOS technologies, as well as high linearity, and large signal bandwidth [7]. However, these characteristics are becoming more difficult to achieve, particularly with low supply voltages. Over the years, MOS transistor dimensions have largely reduced, yet the threshold voltage of CMOS technology is not reduced as expected. Therefore, it is critical for researchers to provide an appropriate and efficient technique for optimizing the design of LV-LP circuits.

One technique that can reduce power consumption is the use of floating gate MOSFETs. Many active components were designed with this technique, including operational amplifiers [8], OTAs [9], differential amplifiers [10], current mirrors [11], and current conveyors [12].

Using a BD input stage is another way to achieve LV and LP operation [13–17].

For conventional MOS transistors, the gate terminal receives the input signal, while the bulk terminal is connected to either the highest or lowest power rails, depending on whether the transistor is PMOS or NMOS. Since the gate input voltage is applied, its value must exceed the threshold voltage (0.5V). However, in a bulk driven MOS transistor, the input voltage is applied to the bulk and the gate is biased to the appropriate voltage. This keeps the transistor operating. The threshold voltage is thus no longer present in the signal path, resulting in a lower supply voltage requirement.

This paper presents a simulation-based technique that we have already tested on the multi-objective optimization of analog circuits, see reference [2, 18], yet here it is adapted for the optimal design of a novel structure of LV-LP bulk driven CCII, using the single-objective particle swarm optimization (PSO) algorithm [19, 20]. This circuit can operate from a V_{DD} of 0.3V, consuming only 37 nW. The ultra-low V_{DD} was achieved by using a non-tailed BD amplifier. In addition, the design has an enhanced bandwidth and can operate without compensation capacitors, even for very high load capacitance. At the same time, accurate voltage and current gain values are being provided.

This paper is organized as follows. Section 2 describes the bulk-driven CCII. Section 3 presents the results and discussions. Section 4 concludes the paper.

2 Bulk Driven Current Conveyor

Fig. 1a shows a positive CCII based on an amplifier operating with unity-gain negative feedback, ensuring $V_X = V_Y$, and $I_Z = I_X$. Fig. 1b shows the transistor level of the BD-CCII. This circuit consists of a X-Y voltage follower part (M1-M3, M5-M8) and a current repetition

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part (M4, M9), creating a current amplifier with unity gain and the Z output terminal of the CCII.

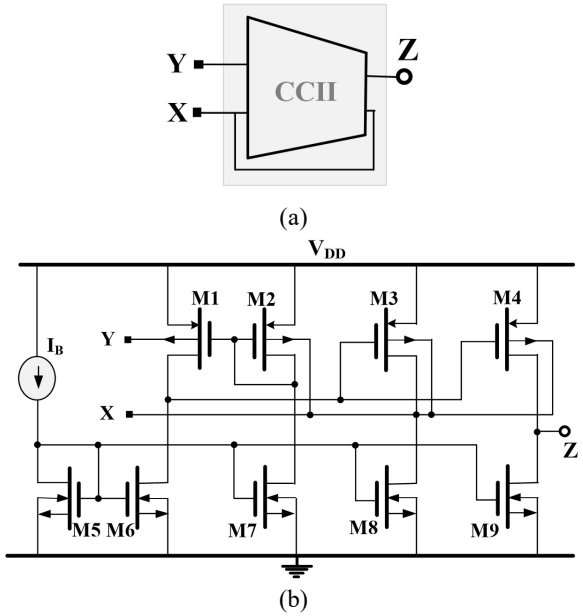


Fig. 1. CMOS Bulk driven CCII Circuit.

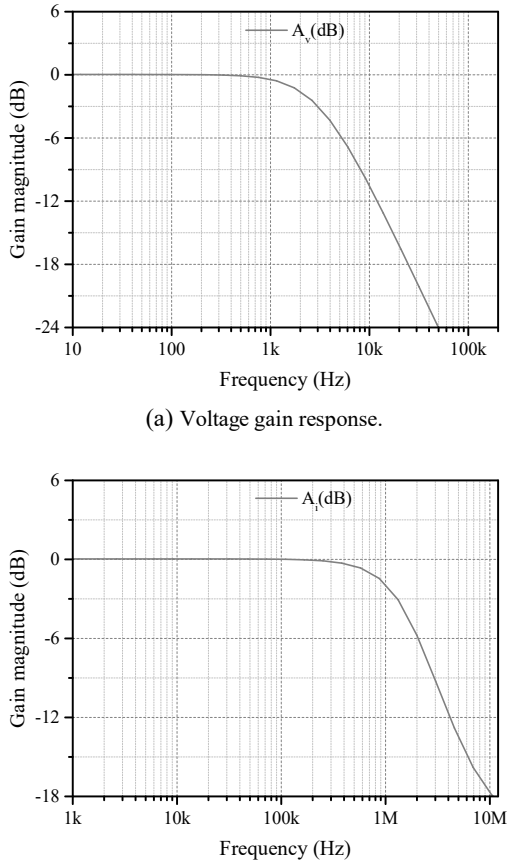
A differential amplifier is formed by the transistors M1-M2 and the current sinks M6 and M7. The second stage of the internal amplifier is made up of the transistor M3 and the current sink M8. The bulks of M2 and M3 are connected together to the amplifier output. Through this connection, a negative feedback loop is closed, which creates a voltage buffer of unity gain. Shorting together the bulks of M2 and M3 ensures that their threshold voltages change with the input signal in the same way. As a result, the voltage gain is more accurate. The internal amplifier would offer poor CMRR performance without this connection. This would decrease the voltage gain accuracy in the voltage follower, making its value greater than 1. It should be mentioned that this circuit can be easily extended to multi-outputs (positive or negative) using cross-coupled current mirror techniques.

3 Simulation results and discussions

We coded the optimization algorithm in C language. The optimization was conducted on an Intel Core i7-7820HQ computer with 2.9GHz and 16G memory. The BD-CCII circuit is discussed and designed using CMOS 0.18 µm process. This circuit was optimized and designed for I_B=2 nA, V_{DD}=0.3V, yet it will also operate with higher V_{DD} and higher bias current (up to 100 nA), resulting in a larger bandwidth. The maximum biasing current depends on the V_{DD}/V_{th} ratio; hence, using a process with a lower V_{th} the current could be increased significantly. Here, the bias current has been obtained for a minimum V_{DD} for the given V_{th} voltages of the used technology.

The transistor's sizes were obtained in µm/µm as: M1,2=20/1, M3,4 = 10×32/1, M5= 20/0.36, M6,7 =10× 34.28/0.36, M8= 10×33.69/0.36 and M9= 10×30/0.36. The ratios W/L are relatively high in order to reduce the VGS voltages of MOS transistors for a given bias current, and to minimize their offset and flicker noise. The channel widths and lengths were determined during the optimization to meet the requirement $|V_{GSi}| \approx V_{DD}/2$ (see Fig. 1, where V_{GSi} denotes the quiescent gate-source voltage of the ith transistor. Hence, this provides the largest possible voltage headroom for process and temperature changes and signal swings.

Fig. 2 present the simulated magnitude response of the current and the voltage follower. The dc gains were +10 mdB (0.999 A/A) and +13 mdB (0.998 V/V), respectively. This shows that a high-accuracy voltage and current follower can be built with relatively LV gain of the internal amplifier and the current repetition circuit (M4, M9).



(a) Voltage gain response.

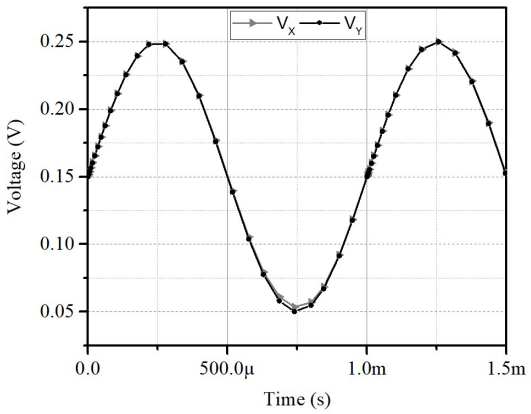
(b) Current gain response.

Fig. 2. Frequency characteristics of BD-CCII, C_L=30pF.

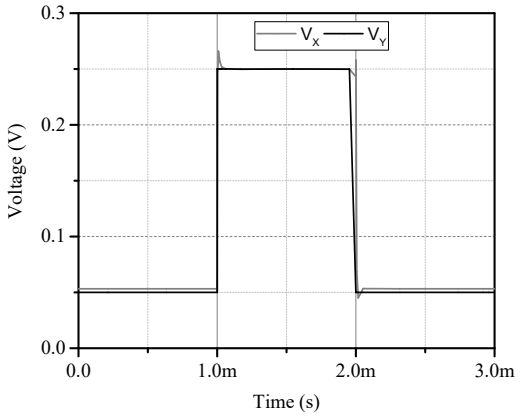
The -3dB bandwidth I_Z/I_X and the -3dB bandwidth V_X/V_Y were 2.28 MHz and 2.79 kHz, respectively. Despite the large capacitance (here 30pF) of this circuit, it can operate without any compensation while remaining precise in both its voltage and current gain values.

The voltage follower sine-wave simulation with the Y input of 200mV and 1kHz frequency is given in Fig. 3a. Fig. 3b presents the step response when a 200mV and a 1kHz square signal were applied to the input (Y terminal). The slew rate SR- and SR+ was 1.3V/ms and 2V/ms, respectively. The SR was mainly limited by the

output stage that is the class A amplifier. This problem can be resolved by a class AB stage.



(a) sine wave response V_X and V_Y.



(b) step response V_X and V_Y.

Fig. 3. BD-CCII transient response.

Fig.4 present the dc characteristic of the circuit as well as voltage error. The error ranged from -33 mV to 11 mV respectively for V_Y ranging from 0 mV to 300 mV.

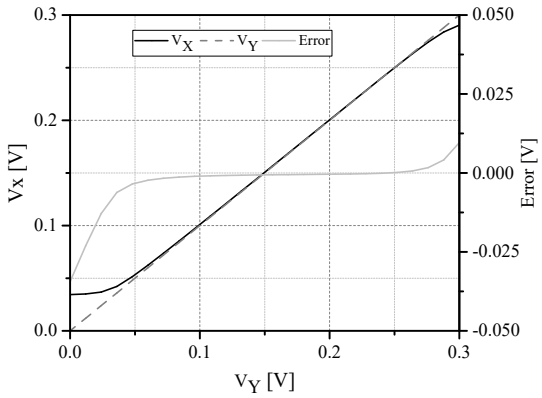


Fig. 3. DC characteristic of the BD-CCII.

Table 1 and Table 2 show respectively the worst-case corners result of the BD-CCII over temperature and process changes. The temperature changes were -10°C, 27°C and 70°C; and the process corners were fast-slow (FS), slow-fast (SF), fast-fast (FF) and slow-slow (SS). The results in those Tables are good confirming the robustness of the optimized CCII over temperature and process analysis.

Table 1. BD-CCII performance analysis over process corners.

Parameter (27°C)	SS	SF	TT	FS	FF
Power [nW]	36.2	36.5	37	37.8	38.9
-3dB bandwidth V_Z / V_X [kHz]	2.45	2.62	2.79	2.83	2.97
-3dB bandwidth I_Z / I_X [MHz]	1.05	1.21	1.3	1.37	1.48
Voltage gain V_Z / V_X [–]	0.998	0.998	0.998	0.999	0.999
Current gain I_Z / I_X [–]	0.998	0.999	0.999	0.999	0.999

Table 2. BD-CCII performance analysis over temperature corners.

Parameter (TT corners)	-10°	27°	70°
Power consumption [nW]	36.0	37	38.5
-3dB bandwidth V_Z / V_X [kHz]	3.00	2.79	2.41
-3dB bandwidth I_Z / I_X [MHz]	1.30	1.28	0.99
Voltage gain V_Z / V_X [–]	0.998	0.998	0.999
Current gain I_Z / I_X [–]	0.999	0.999	0.999

Table 3 gives the obtained results of the circuit for V_{DD} = 0.3 V and its comparison with the previously published. The studied circuit and the one in reference [22] offer the lowest supply voltage and the highest V_{th}/V_{DD} and V_{in-max}/V_{DD} ratios. The presented circuit also offers the lowest bias current and the highest slew rate and R_Z resistance.

Table 23. BD-CCII performance analysis over process corners.

Parameter	This work	[12]	[21]	[22]	[23]
CMOS technology [µm]	0.18	0.18	0.18	0.18	0.18
Supply voltage [V]	0.3	±0.5	±0.4	0.3	0.5
Bias current [nA]	2	–	–	2.5	–
Power consumption [nW]	37	10E3	64E3	19	30E3
Slew rate [V/ms]	2.7	–	–	2	–
Input resistance R_X [Ω]	52E3	42	27	56E3	260
Resistance R_Y [MΩ]	743	≈ ∞	≈ ∞	703	≈ ∞
Resistance R_Z [MΩ]	112	53	0.89	94.7	0.113
-3dB bandwidth V_Z / V_X [kHz]	2.79	4.8E3	14E3	4.1	11E3
-3dB bandwidth I_Z / I_X [MHz]	1.28	8.2E3	13E3	39.2	10E3
Voltage gain [V / V]	0.999	1	1	0.999	0.996
Current gain [A / A]	0.999	1	1	0.9987	0.998
100*(V_{th}/V_{DD})[%]	166	50	62	166	100
100*($V_{in,max}/V_{DD}$)[%]	100	100	95	100	80

The -3dB frequency of the current gain was considerably larger than the -3dB bandwidth of the voltage gain, as expected. Note that the larger V_{DD} increases the bandwidth of both gains, as larger bias currents are possible. Hence, using a process with lower V_{th}, a much higher bandwidth could be achieved with the same structure. In addition, cascode connections could be used, which increases the circuit accuracy. Such a CCII design is suitable for biomedical applications in which the frequency ranges of signals ranging from sub-hertz up to 10 kHz and the LV LP consumption are the main concern.

4 Conclusion

This paper discusses the design and optimization of an ultra-low voltage and low power bulk-driven CCII. The optimized circuit is simple, compact and able to operate at 0.3 V, with a consumption power of 37 nW . The extremely low power supply was achieved with a non-tailed BD differential stage amplifier. In spite of high load capacitances, this circuit provides high current and voltage gains accuracy without using any compensation, thereby allowing circuit area to be reduced. In typical conditions as well as in the process/temperature corners, the circuit has shown excellent performances. Compared to previous works, the optimized circuit provides better ratios V_{th}/V_{DD} and V_{in-ma}/V_{DD}, slew rate, -3dB bandwidth, and bias current, within a compact and reliable structure.

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