Modeling and Analysis of Carbon-Nanotube Interconnections for Future Nanotechnology Interconnections between High Speed CMOS Integrated Circuits using FDTD Method

Nadir Youssef [1,2], Belahrach Hassan [2,3], Ghammaz Abdelilah [3], Naamane Aze-eddine [1,2] and Radouani Mohammed [1]

[1] L2MC Laboratory, National School of Arts and Crafts, Morocco, Meknes
[2] Electrical Laboratory, Royal School of Aeronautics, Morocco, Marrakech
[3] Laboratory LSEEET, University Cadi Ayyad, Morocco, Marrakech

Abstract. The size reduction of copper interconnects degrades their performances due to increased surface scattering, which significantly reduces the effective electron mean free path. Unlike Cu, CNTs support ballistic electron flow with a lower value of mean free, which highly induces researchers to change copper by carbon nanotubes. In this way, this paper presents an accurate method based on the finite difference method describing the behavior of carbon nanotube interconnects in the time domain. The proposed algorithm is implemented in the MATLAB tool. The crosstalk between the interconnects and the induced delays are studied as a function of their length and the technology node (45nm, 32nm, 22nm and 16nm). The values obtained by the suggested method are compared with those of the PSPICE simulation tool. A good agreement between these results is observed, which demonstrates that CNT interconnects are more efficient than copper ones in terms of crosstalk induced delays.

1 Introduction

With the increasing demand for high speed signals and the reduction in component size, interconnect effects, for instance, signal delay, crosstalk and distortion are becoming the main limits for the high speed systems performances. However, at the global interconnect level, most conventional materials such as aluminum and copper are impacted by the electromigration effect due to high current density. In this context, this paper is devoted to the study of CNTs based interconnects for upcoming CMOS integrated circuit interconnects in nanotechnology. Given that, with the downscaling of CMOS and higher clock frequency, the need of higher frequency bandwidth and lower resistance are the main concerns in interconnects' design. While the performance of copper being restrained by dispersion, signal degradation, skin effect, power electromagnetic interference and dissipation [1]. Therefore, the exploration and research of alternative materials for on-chip interconnect lines are essential and necessary for future high performance and low power chips. Thus, a lot of research on nanoribbon graphene (GNR) and carbon nanotube (CNT) is being conducted for applications focusing on microelectronic devices and interconnects. These technologies have been investigated as promising candidates to replace field effect transistor channels and interconnects for next-generation very large integrated circuits. These studies are based on the possibility to replace Cu interconnects by CNTs and also to satisfy both high performance and low power consumption [2].

In the current state of the nanoscale, interconnects are classified into three layers according to their length: global, intermediate and local. The two first layers of interconnects from the substrate are considered local, the intermediate are assumed to be the third and fourth layers, and global are the upper layers. In addition, metal vias are used to connect the interconnects from one level to another [3]. Local interconnects are narrow lines fastening transistors and gates within a processing unit or functional block on the integrated circuit. Furthermore, local interconnects occupy a first and ocasionally a second layer in a multi-level system. And over the years, the interconnections length tends to decrease according to technological advancement: 45nm, 32nm, 22nm, 16nm.

Carbon nanotubes (CNTs) are known by their unique band structure and atomic arrangement that are behind their exceptional mechanical and electrical properties. Today, the extraordinary properties of CNTs lead to consider them as the most vaunted nano-interconnect materials. The electrical properties of CNTs depend mainly on their chirality. Many theoretical studies have established that they have a high electrical conductivity. However, energy band modelling confirms one of the important characteristics of CNTs: their metallic or semiconducting behavior, depending on their diameter and chirality. The particular structure of the nanotubes suggests that their conductivity must also be important along the CNT axis [4].

In this work, we present how the electrical parameters of CNTs vary when the number of walls increases, the type of CNT changes in a mixed bundle and as a function of length. However, the present paper we overview the following section: in the first one, a modeling of the electromagnetic coupling between MWCNT interconnects bundles has been presented. Secondly, an examples and analysis when we compare between the propagation delays of the two technologies Cu and CNT. And finally, the conclusion.

2 Modeling the electromagnetic coupling between MWCNT interconnect bundles

MWCNT bundles have potentially shown interesting performances in current very large scale integration (VLSI) nano-interconnects. From a fabrication viewpoint, it is hard to master the growth of a dense bundle containing MWCNTs with equal diameters. However, a realistic bundle is a mixture of MWCNTs with a different number of walls. Thus, this section concentrates on the modeling of a bundle composed by MWCNTs characterized by different number of walls and diameters (called mixed MWCNT bundle (MMB)). Moreover, according to the theory of multiconductor transmission lines (MLT), an equivalent single conductor model (ESC) is used for an MMB arrangement. This model allows the comparison of the dynamic crosstalk delay between MMB structures and conventional bundle structures composed by several MWCNTs with equal diameters (MWCNT (MB) bundle) as a function of length and node technologies [5].

2.1 ESC model based on geometry

This subsection shows several arrangements of MWCNTs in a bundle which can be dependent on the MWCNT geometry. Initially, a model of the multiconductor transmission lines (MTL) of the MWCNT bundle is used to get the interconnect elements namely capacitance [C], resistance [R] and inductance [L] per unit length [6]. The geometry of the MWCNT over the ground at a distance h is shown in Figure 1, which includes various concentric rolled graphene walls of diameters $d_1, d_2, ..., d_n$.
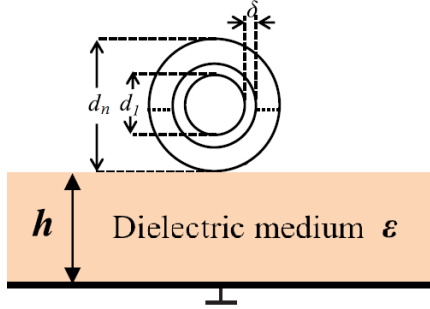

Fig. 1: Individual MWCNT interconnect above the ground plane.

In the existing CNT technology, the interwall spacing is equal to the Van-Der-Wall distance ($\delta \simeq 0.34 \, nm$) and can be expressed as [6]:

$$\delta = \frac{d_i - d_{i-1}}{2} \qquad (1)$$

The outer diameter d_n of MWCNT can be written as:

$$d_n = d_1 + 2 \times \delta \times (n-1) \qquad (2)$$

Where the inner wall is represented by d_1, and n represents the total number of walls.

In Figure 2, we present two different conventional and mixed bundle arrangements of CNT interconnects [6].
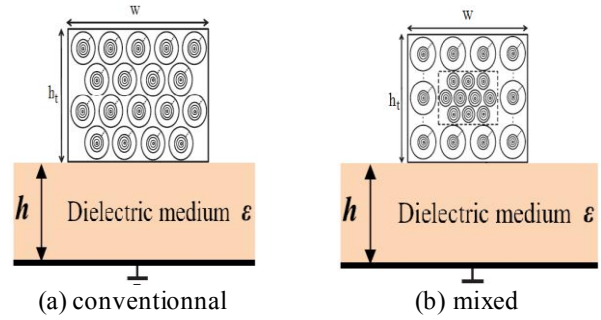

(a) conventionnal (b) mixed

Fig. 2 : Configurations of MWCNT bundle

The total number of MWCNTs relative to the height (h_t) and width (w) of the bundle can be written as [7]:

$$N_{MWCNT} = \left[N_W N_{h_t} - int \left[\frac{N_{h_t}}{2} \right] \right] \qquad (3)$$

where int[.] represents an integer value, N_W and N_{h_t} represent respectively the number of MWCNTs in width (W) and height (h_t), and are expressed as [8]:

$$N_W = 1 + \frac{W - d_n}{d_n + \delta} \quad \text{and} \quad N_{h_t} = 1 + \frac{h_t - d_n}{(d_n + \delta)\sqrt{3}/2} \qquad (4)$$

To find an equivalent electrical model of a conventional or mixed CNT bundle we need the electrical model of each wall of the MWCNT. The combination of these models allows to obtain a single equivalent electrical model (ESC) of the MWCNT bundle. Indeed, the ESC model supposes that whole walls of the MWCNT and whole MWCNTs in a bundle are parallel and contribute in the conduction. The tunneling conductance G_t which mainly represents the inter-wall and inter-CNT electron tunneling effects can be neglected in the ESC model due to the negligible interaction between two walls of a MWCNT [9]. Nevertheless, each MWCNT bundle has three main parasitic elements resistance [R_{ESC}], capacitance [C_{ESC}] and inductance [L_{ESC}] per unit length as depicted in figure 3.
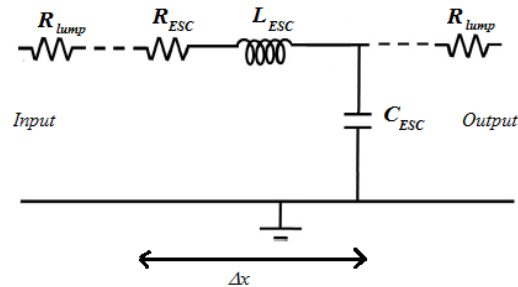

Fig. 3: Equivalent circuit ESC model of MWCNT

The equivalent resistance of the ESC model is written as [10,11]:

$$R'_{ESC} = R_{lump} + R_{ESC}l \qquad (5)$$

where

$$R_{lump} = \left[\left(\frac{1}{(N_{MWCNT})_{m_1}} \left(\frac{R_q}{\sum_{i=1}^{n_1} N_i} + R_{mc} \right) \right)^{-1} + \right.$$
$$\left. ... + \left(\frac{1}{(N_{MWCNT})_{m_k}} \left(\frac{R_q}{\sum_{i=1}^{n_k} N_i} + R_{mc} \right) \right)^{-1} \right]^{-1} \qquad (6)$$

$$R_{ESC} = \left[\left(\frac{1}{(N_{MWCNT})_{m_1}} \left(\frac{R_q}{\sum_{i=1}^{n_1} N_i \lambda_{mpf,i}} \right) \right)^{-1} + \cdots + \right. \qquad (7)$$

$$\left(\frac{1}{(N_{MWCNT})_{m_k}}\left(\frac{R_q}{\Sigma_{i=1}^{n_k} N_i.\lambda_{mpf,i}}\right)\right)^{-1}\Bigg]^{-1}$$

R_q represent quantum or intrinsic resistance;

R_{mc} represent resistance of imperfect nanotube-metal contact;

N_i represents the conducting channels number in i^{th} MWCNT wall;

$\lambda_{mpf,i}$ represent the mean free path for i^{th} wall present in the MWCNT structure;

$m_1, m_2, \ldots, m_k$ are the various types of MWCNT in the bundle;

n_k is the walls' number in the kth type of MWCNT;

l is the interconnect length;

The equivalent capacity of the ESC model in Figure 3 is composed of [10,11]:

$$C_{ESC} = \left(1/C_{Q,ESC} + 1/C_{E,ESC}\right)^{-1} \tag{8}$$

Where

$$C_{Q,ESC} = \frac{2e^2}{hv_F} \times [(N_{MWCNT})_{m_1} \sum_{i=1}^{n_1} N_i + \\ \ldots (N_{MWCNT})_{m_k} \sum_{i=1}^{n_k} N_i] \tag{9}$$

and

$$C_{E,ESC} = \frac{2\pi \varepsilon_0 \varepsilon_r}{cosh^{-1}\left[\left(\frac{(d_n + 2h)}{d_n}\right)\right]} \times N_W \tag{10}$$

where h and e are respectively the Planck's constant and the electron charge; and v_F is the Fermi velocity.

The inductance of the ESC model is expressed as [10,11]:

$$L_{ESC} = L_{K,ESC} + L_{M,ESC} \tag{11}$$

$$L_{K,ESC} = \left[\left(\frac{1}{(N_{MWCNT})_{m_1}}\left(\frac{L_K}{\Sigma_{i=1}^{n_1} N_i}\right)\right)^{-1} + \cdots + \right.$$

$$\left.\left(\frac{1}{(N_{MWCNT})_{m_k}}\left(\frac{L_K}{\Sigma_{i=1}^{n_k} N_i}\right)\right)^{-1}\right]^{-1} \tag{12}$$

$$L_K = \frac{h}{2e^2 v_F} \tag{13}$$

$$L_{M,ESC} = \frac{\mu_0}{2\pi} cosh^{-1}\left(\frac{d_n + 2h}{d_n}\right) \tag{14}$$

2.2 Analysis of electromagnetic coupling in mixed CNT bundle using FDTD method

Consider N CNT interconnect lines as shown in figure 4, modeled by the following system of coupled partial differential equations (Telegrapher's equations) [12]:

$$\begin{cases} \frac{\partial}{\partial x}\mathbf{V}(x,t) + \mathbf{R}_{ESC}\mathbf{I}(x,t) + \mathbf{L}_{ESC}\frac{\partial}{\partial t}\mathbf{I}(x,t) = \mathbf{0} \\ \frac{\partial}{\partial x}\mathbf{I}(x,t) + \mathbf{C}_{ESC}\frac{\partial}{\partial t}\mathbf{V}(x,t) = \mathbf{0} \end{cases} \tag{15}$$

Where the currents **I** and voltages **V** are written in Nx1 column vector form, and interconnect parameters $\mathbf{R}_{ESC}$, $\mathbf{L}_{ESC}$ and $\mathbf{C}_{ESC}$ are expressed in NxN matrices per unit length.
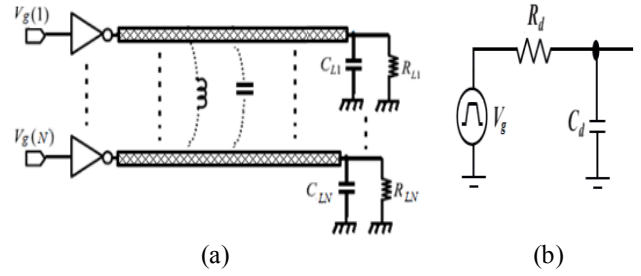

(a)   (b)

Fig. 4: (a) N-interconnect coupled MWCNT with drivers and loads, (b) CMOS inverter model

In this work we will present the Finite Difference method in the Time Domain (FDTD) to solve the equations system (15). This method is based on the discretization of the spatial domain into Nx cells each of length Δx, and the time domain into Nt intervals each of duration Δt. This discretization uses an interlaced leap-frog scheme such that the currents are computed at (t+Δt/2) steps and (x+Δx) positions, whereas the voltages are computed at (t+Δt) steps and (x+Δx/2) positions. From the system of equations (15) we can calculate the current and voltage at any point on the interconnect lines MWCNT by:

For k=2,3, … Nx

$$V_{k+1/2}^{n+1} = V_{k+1/2}^n + A[I_{k-1}^{n+1/2} - I_k^{n+1/2}] \tag{16}$$

For k=1,2,3, … Nx

$$I_k^{n+3/2} = BDI_k^{n+1/2} + B[V_{k+1/2}^{n+1} - V_{k-1/2}^{n+1}] \tag{17}$$

Where A, B and D are square matrices NxN dependent on the line parameters R_{ESC}, L_{ESC} and C_{ESC}:

$$A = \left[\frac{\Delta x}{\Delta t} C_{ESC}\right]^{-1}; B = \left[\frac{\Delta x}{\Delta t} L_{ESC} + \frac{\Delta x}{2} R_{ESC}\right]^{-1}; D = \left[\frac{\Delta x}{\Delta t} L_{ESC} - \frac{\Delta x}{2} R_{ESC}\right]$$

To find out the currents and voltages at the extremities of the structure investigated, the nature of the load circuits must be taken into account. The voltage and current at the near extremity are expressed by V_1 and I_0 respectively. It is noticed that to apply the boundary conditions of equation (16), Δx must be replaced by Δx/2. Thus, at k=1 equation (16) becomes:

$$V_1^{n+1} = EV_1^n + 2A[G_{lump}V_0^{n+1} - I_1^{n+1/2}] \tag{18}$$

With

$$V_0^{n+1} = F\left[\frac{1}{\Delta t}C_d V_0^n + G_d V_g^{n+1} + G_{lump}V_1^{n+1}\right] \tag{19}$$

where $G_{lump} = (R_{lump})^{-1}$, $G_d = (R_d)^{-1}$,

$E = [U + 2AG_{lump}]^{-1}$, $F = \left[G_d + G_{lump} + \frac{1}{\Delta t}C_d\right]^{-1}$

The voltage at k=Nx+1 is given by:

$$V_{Nx+1}^{n+1} = EV_{Nx+1}^n + 2EA\left(\frac{1}{2}G_{lump}V_{out}^{n+1} + I_{Nx}^{n+1/2} - \frac{1}{2}I_{out}^n\right) \tag{20}$$

The output voltage and current are given by:

$$V_{out}^{n+1} = QV_{out}^n + \Delta t C_L^{-1} G_{lump} V_{NDX+1}^{n+1} \tag{21}$$

$$I_{out}^{n+1} = G_{lump}\left(V_{NDX+1}^{n+1} - V_{out}^{n+1}\right) \tag{22}$$

where $Q = U - \Delta t C_L^{-1} G_{lump}$ with U is a unit matrix.

Of these equations, the voltages and currents along the line are evaluated during a specific time of the equations in terms of previous voltage and current values. Nevertheless, the FDTD method gives a near-accurate resolution if the following conditions are met:

-The spatial increment step Δx must be small enough relative to the wavelength to achieve good spatial resolution.

-The time step Δt must be small to ensure the CFL stability condition [12].

The relationships of the voltage and current at input, output and along the line interconnects are implemented in MATLAB. Some examples will be studied in the following section.

3 EXAMPLES AND ANALYSIS

3.1 Comparison between the propagation delays of the two technologies Cu and CNT

In order to validate the reason for replacing Cu with CNT as already mentioned in the introduction, it is necessary to make a comparison between the delays associated with Cu and CNT interconnects. This was one of the factors limiting the performance of Cu interconnects. To do this, we performed a modeling on MATLAB by integrating the proposed algorithms as well as the different values of the electrical parameters R, L, C for different technologies as a function of the length to know the delay of the output voltage of the interconnect. This delay is obtained by measuring the time needed to reach half of the maximum of the output signal. The MATLAB results as a function of technology node and length for Cu and CNT are summarized in the table below.

Table 1: Interconnection output delay for Cu and CNT results.

Delay (ps)	Cu 45nm	CNT 45nm	Cu 32nm	CNT 32nm
$l=100\mu m$	74,69	14,76	167,4	15,19
$l=200\mu m$	81,99	16,13	183,7	17,78
$l=300\mu m$	104,7	18,09	214,3	21,16
$l=400\mu m$	122,5	20,17	264,1	24,73
$l=500\mu m$	142,4	22,61	299	29,44
$l=600\mu m$	156,4	25,83	328,6	34,81
$l=700\mu m$	175,4	28,83	362,9	40,03
$l=800\mu m$	199,4	32,11	389,8	46,67
$l=900\mu m$	209	35,72	442,7	52,91
$l=1000\mu m$	224,5	40,25	492,8	60,76
Delay (ps)	Cu 22nm	CNT 22nm	Cu 16nm	CNT 16nm
$l=100\mu m$	430,2	16,76	1056	19,66
$l=200\mu m$	479,5	22,06	1126	28,69
$l=300\mu m$	545,8	28,18	1252	40
$l=400\mu m$	615,0	36,31	1388	52,91
$l=500\mu m$	719,2	45,1	1524	68,45
$l=600\mu m$	823,6	58,13	1665	86,66
$l=700\mu m$	915,1	68,06	1820	108
$l=800\mu m$	1016	80,58	2016	129,6
$l=900\mu m$	1110	95,1	2262	155,6
$l=1000\mu m$	1196	112,6	2514	181,1

We can observe from Table 1 that the propagation delays through the interconnects increase with increasing length and decreasing technology node for each material. In addition, the Cu-based interconnect delay increases more significantly by the order of tens than that of CNT due to the high resistance of copper.

3.2 Crosstalk induced delay in MWCNT

In this subsection, we focus on a coupled three-line MWCNT system where the parameters RESC, LESC, and CESC are calculated from the relationships described above. The circuit corresponding to this configuration is shown in Figure 5.
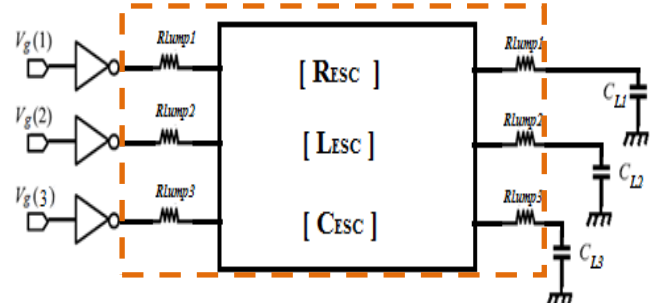

Fig. 5: Example of a three interconnect MWCNT structure test circuit.

The MWCNT interconnect lines are excited with step signals with rise time T_r=20ps and amplitude V_a= 0.9V. The length of the lines for the reference configuration is l= 1mm and the observation time is fixed to t_{stop}= 0.5ns. Load capacitive C_L=1fF.

In this three coupled line system, we consider respectively line 1 as aggressor, line 2 as victim and line 3 as aggressor in order to observe the induced voltage at the output of line 2. Thus different cases of input signal switching are analyzed to compare the propagation delays for different states of the excitation sources.

After obtaining the input and output voltage recurrence relations, we implemented them on MATLAB. Also simulated the structure with the PSPICE tool. The obtained results are grouped on the following tables.

Table 2: Time delays at second line MATLAB and PSPICE results.

Type mode	Line-1 (Agressor)	Line-2 (Victim)	Line-3 (Agressor)
Type- 1	0→1	0→1	0→1
Type- 2	0→1	0→1	Gnd
Type- 3	0→1	0→1	1→0
Type- 4	1→0	0→1	Gnd
Type- 5	1→0	0→1	1→0
Type mode	**Delay line-2 Proposed method**	**Delay line-2 PSPICE**	**Relative error (%)**
Type- 1	44,77ps	43,1ps	3,7
Type- 2	52,63ps	50,15ps	4,7
Type- 3	80,45ps	78,13ps	2,88
Type- 4	93,85ps	91,92ps	2,06
Type- 5	110,3ps	108,68ps	1,47

Table 2: Crosstalk amplitude at second line MATLAB and PSPICE results.

Crosstalk amplitude (mV)	Proposed method	PSPICE results	Relative errors (%)
l=0.2mm	63,919	61,35	4
l=0.5mm	72,763	70,7	2,8
l=1mm	98,599	96,05	2,58
l=1,5mm	122,82	119,4	2,78
l=2mm	127,2	125,3	1,5

As a conclusion, we found a good agreement between the two results obtained by the MATLAB and PSPICE tools. This proves the accuracy of our model.

4 CONCLUSION

Based on the FDTD method, we have modeled and simulated the crosstalk induced delays of mixed interconnect MWCNT, using the telegrapher's equations. The proposed algorithm is implemented on MATLAB. After the comparison between the resulted values and the PSPICE simulations, a good agreement between those results is observed. The proposed algorithm has been validated numerically with different examples. This study shows that CNT interconnects are able to conduct a large current through a small cross-section and meanwhile avoiding the signal degradation and the electromigration problems that are usual in copper interconnects. Also, the resistance of bundled CNTs is around three times lower than that of individual CNTs. Thus, it is expected that CNT bundles will emerge as an alternative for copper replacement either for interconnects and for VLSI chips vias in future.

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