Performance evaluation of SRAM design using different field effect transistors

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Abstract. SRAM (Static Random Access Memory) is one of the type of memory which holds the data bit without periodic refreshment. Compared with DRAM (Dynamic Random Access Memory) which requires periodic refreshment of data bit stored in it. Unlike Dynamic RAM, Static RAM uses a flip-flop circuit to store each data bit, whereas Dynamic RAM uses a capacitor to store the data bit. But capacitor has tendency of losing charge which requires periodic refreshment. Thus SRAM perform better and have more stability than DRAM especially in idle state. In this work, we analysed the performance of the SRAM cell which are built with different field effect transistors and calculated the Write and Read delays, PDP (Power Delay Product) and Static Noise Margin (SNM) for all types of transistors. SRAM cell which is based on the CNT technology with optimized parameters of CNT density, CNT diameter and CNTFET flat band voltage has the better performance and stability compared with other device technologies. Optimized CNTFET SRAM cell compared with the MOSFET based SRAM the write and read delays are improved by 85.8% and 94.3% respectively. All the simulations have been carried out using HSPICE tool for 32nm technology node.

Keywords
SRAM, CNTFET, DRAM, FINFET, GNRFET.

1 Introduction

Mostly SRAM cells are built with MOSFET, but as the channel length of the MOSFET enters into the nano-meter range the short channel effects will threatens the performance of

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the SRAM. To Overcome these short channel effects, we can opt the different type of field effect transistors in place of the MOSFET, CNTFET and FINFET.CNTFET(Carbon Nano Tube Field Effect Transistor) is a type of transistor that uses the carbon nanotubes as channel material instead of semiconductor material like silicon [1-3]. In CNTFET, the CNT(Carbon Nano Tube) serves as the semiconductor channel between the source and the drain terminals similar conventional MOSFETs as shown in Fig 1. These Carbon Nano Tubes are made of carbon atoms that are arranged in two-dimensional honey-comb lattices. CNTFETs have potential to revolutionize the field of electronics and enable the development of new technologies that are not possible with traditional silicon based devices [4-7].

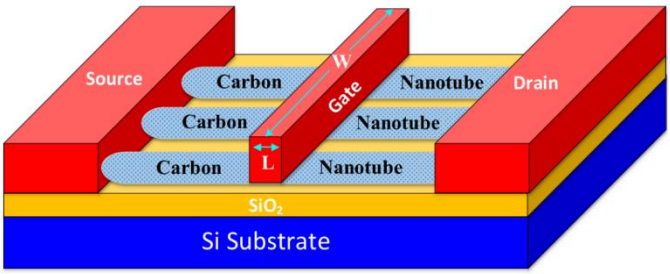

Fig 1.Carbon Nano Tube Field Effect Transistor.

A FinFET (Fin Field-Effect Transistor) is a type of 3D transistor that is widely used in modern electronic devices and many other digital systems. In planar FET the Gate is placed above the channel and there is leakage current flowing from the source to drain when the gate is off. But in FinFET the channel is thin vertical fin and gate is wrapped around it as in Fig 2. This help in better controlling of the channel and thus reducing the leakage current and improving the electrical properties. FinFETs, however, are highly scalable, meaning that they can be manufactured at increasingly smaller process nodes, allowing for higher transistor density and improved performance [8-12].

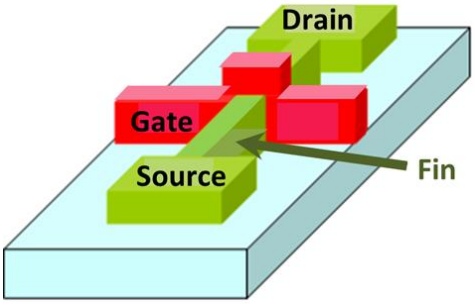

Fig 2: Fin Shaped Field Effect Transistor.

GNRFET (Graphene Nanoribbon Field-Effect Transistor) is a type of transistor that uses graphene nanoribbon as the channel [13-15]. Graphene nanoribbons are narrow strips of graphene, a single layer of carbon atoms arranged in a hexagonal lattice structure. GNRFETs have several advantages over other types of transistors and that consume low power and have high performance compared to MOSFET. This makes GNRFET a promising technology for future electronic devices due to their unique properties and high performance applications[16-23].

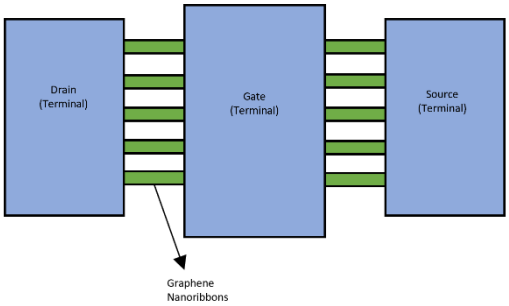

Fig 3:Graphene Nano Ribbon Field Effect Transistor.

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2 SRAM design and operation

SRAM (Static Random Access Memory) is a type of memory cell used in many digital applications. It is called "static" because it does not require periodic refresh cycles to maintain its contents, unlike Dynamic RAM (Random Access Memory), which requires a constant refresh.

The 6T SRAM cell consists of six transistors in which four transistors are arranged in a cross-coupled latch configuration. The two cross-coupled inverters store the binary value of 0 or 1, and the two access transistors provide read and write access to the cell. These access transistors are controlled by a word line, which is used to select the cell for read or write operations.

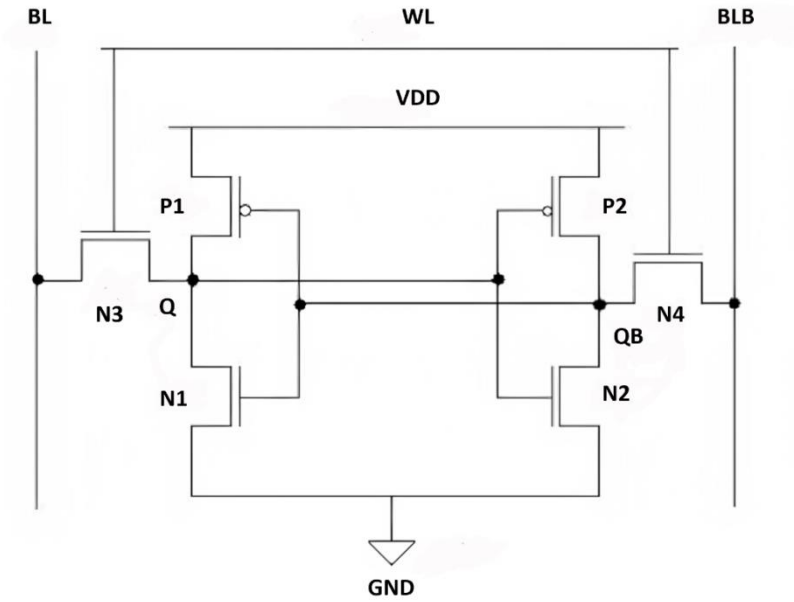

Fig 4: Schematic of 6T SRAM Cell

Write Operation:

Let assume that memory cell has to hold bit one which means Q=1 and QB=0.Apply high voltage to write line i.e., (WL=1).Then Supply high voltage (1v) to BL and low voltage (0v) to BLB. The voltages that we applied through BL and BLB will get to Q and QB then the data bit will continuously latch between two cross coupled inverters. And make write like as low then hold of bit takes place.

Read Operation:

Let assume that memory is already holding bit one i.e., (Q=1 and QB=0).In order to perform read operation we should make word line as high (WL=1).Now voltage from the Q will flow into BL and QB will flow into BLB.BL and BLB terminals are connected to sense amplifier which gives amplified differential voltage between BL and BLB. By observing the output voltage from the sense amplifier, we can identify the data that is stored in SRAM cell.

Hold Operation:
To perform the hold operation we should make the word line as low (WL = 0). Then the data bit we stored in the SRAM cell will continuously latch up in the cross coupled inverters.

3 Simulation results

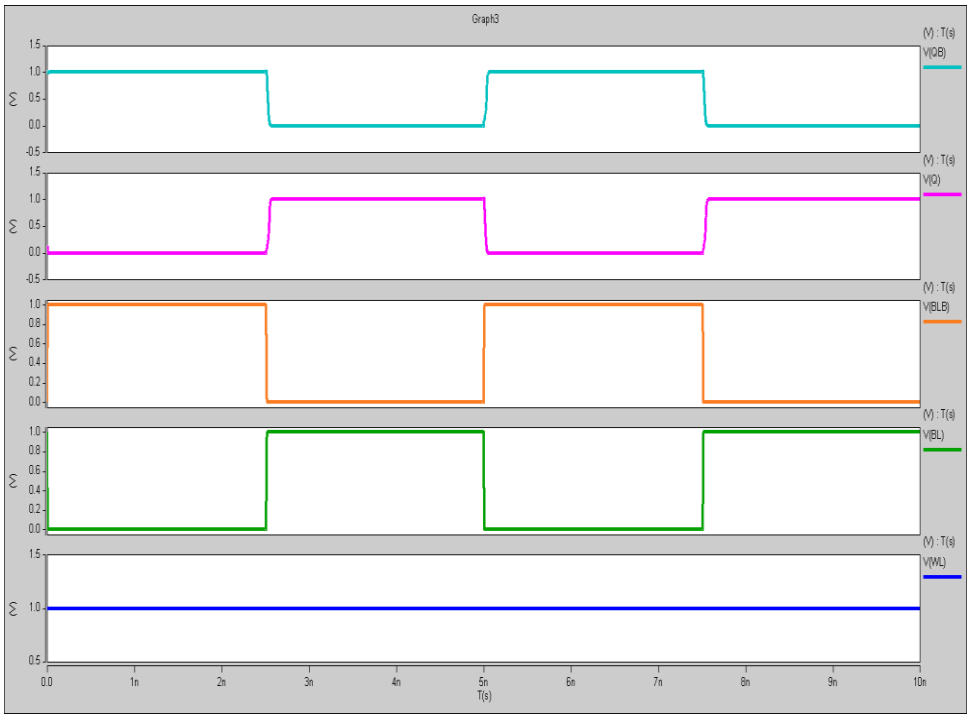

Fig 5. Write Operation Of 6T SRAM

Here are the simulation results of the 6T SRAM which is basically built with 32nm CMOS technology and comparison of performance metrics of the 6T SRAM which are built with different FETs (Field Effect Transistors).

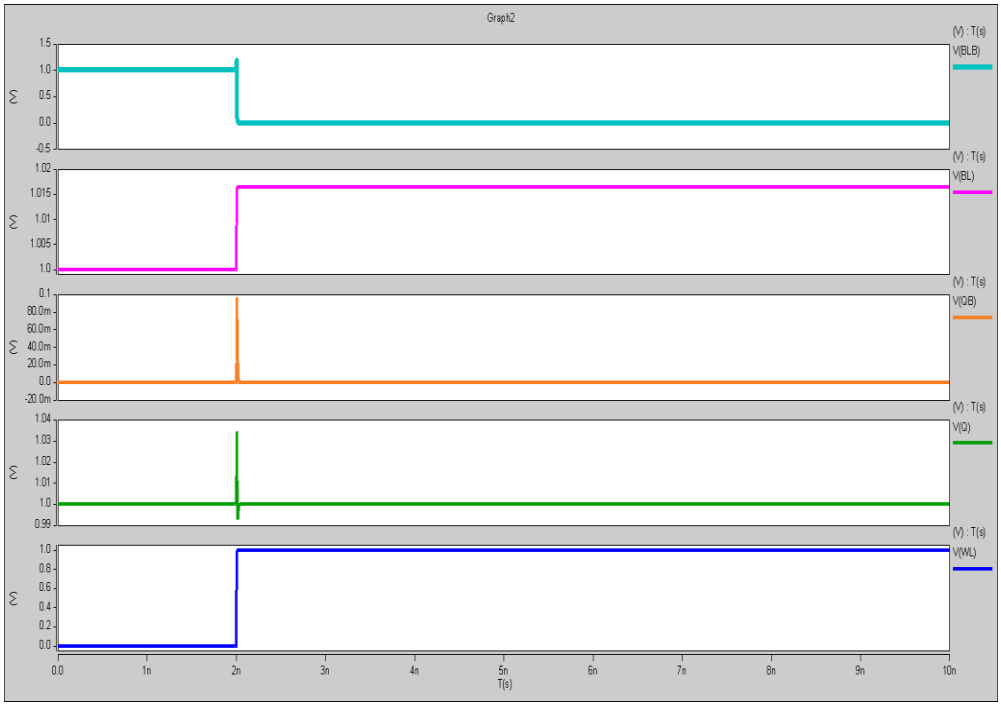

Fig 6. Read Operation Of 6T SRAM.

By observing the Table 1 we can conclude that CNTFET has the lower read and write delays compared with different field effect transistors. The power dissipation of different Field Effect Transistor during the read and write operation is interpreted in Table 1. Other than the MOSFET different FETs have the lower power dissipation. Power Delay Product (PDP) is a metric used to measure the efficiency of digital circuit. It is defined as the product of the power consumed by the circuit and delay of the circuit. Table 1 consists the read and write PDPs of the different field effect transistors.

Table 1: Read, write delays and power analysis of SRAM using different Field Effect Transistors

Different FETs	Write Delay(ps)	Read Delay(ps)	Write Power(uw)	Read Power(uw)	Write PDP(W.s)	Read PDP(W.s)
MOSFET	30.15	5.12	19.04	0.98	5.07E-16	5.05E-16
FINFET	10.11	2.52	0.43	0.014	7.66E-18	7.01E-19
GNRFET	4.32	2.50	0.10	0.014	9.65E-19	3.80E-20
CNTFET	4.29	0.27	0.45	0.022	4.33E-19	6.07E-21

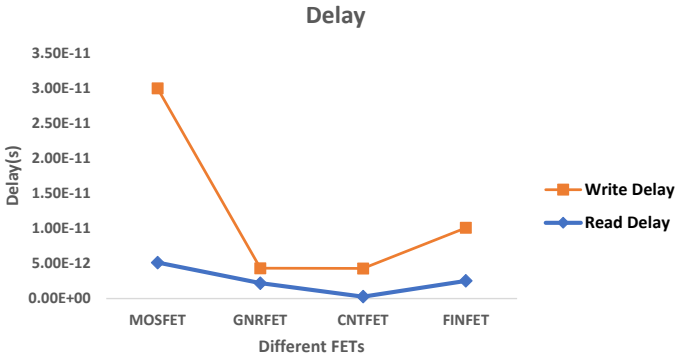

Fig7: Read, write delay analysis of SRAM using different Field Effect Transistors.

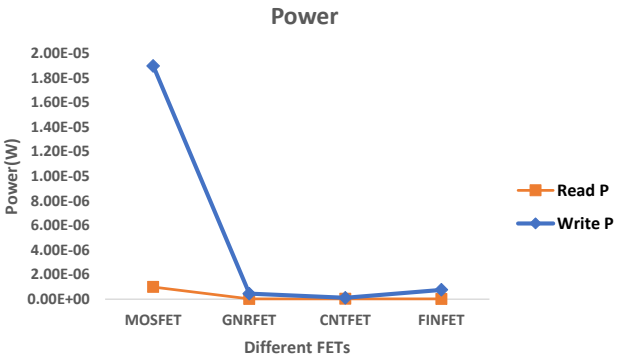

Fig 8: Read, write power analysis of SRAM using different Field Effect Transistors.

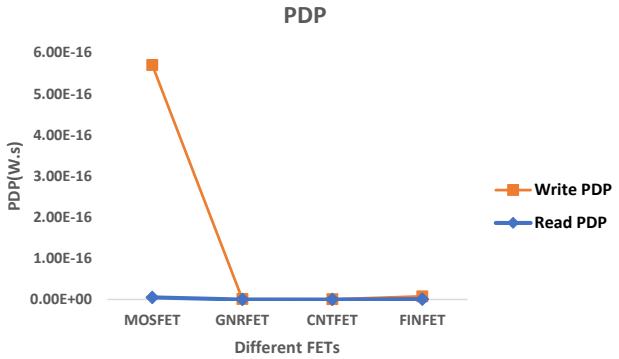

Fig 9: Read, write power delay product analysis of SRAM using different Field Effect Transistors.

Static Noise Margin(SNM) is a measure of the sensitivity of a SRAM cell to noise. Hold SNM represents the ability of SRAM to retain the stored data in absence of word line. Write SNM refers the minimum voltage required to feed new value into SRAM cell and Read SNM refers to the ability to prevent the SRAM cell to flip the stored value while

stored value is being read. Hold, Read and Write SNMs of 6T SRAM which are built with different FETs are interpreted into Table 2.

Table 2: Hold, Write and Read SNMs of 6T SRAM with Different Field Effect Transistors.

Different FETs	Hold SNM(V)	Read SNM(V)	Write SNM(V)
MOSFET	0.45	0.41	0.11
FINFET	0.36	0.72	0.14
GNRFET	0.35	0.55	0.17
CNTFET	0.30	0.52	0.20

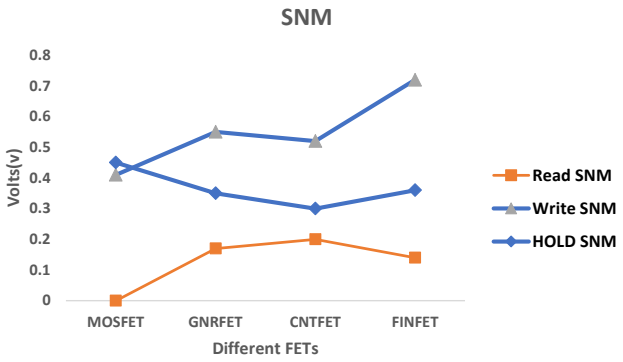

Fig 10: Hold, Write and Read SNMs of 6T SRAM with Different Field Effect Transistors.

Among the different FETs, CNTFET has less read and write delays, power dissipation and has the marginal SNM. We can also improve the performance of the SRAM by adjusting the different parameters of CNTFET i.e.. diameter of the CNT (Dcnt), Number of the CNT tubes (Ncnt) and flat band voltage(Vfb).As the diameter of the CNT (Dcnt) increases the read and write delays of the SRAM will decreases. This is because larger diameter of CNTs has the lower resistance and capacitance, which allows the transistor to have faster switching speed. Read and Write Delays of the CNTFET SRAM by varying the diameter of the CNTs are interpreted in Table 3.

Table 3: Write and read Delays of SRAM by varying the diameter of CNT.

Diameter of CNT(nm)	Write Delays(ps)	Read Delay(ps)
1nm	4.51	1.92
2nm	4.15	3.32
3nm	4.32	3.85
4nm	3.85	4.09
5nm	3.78	4.38

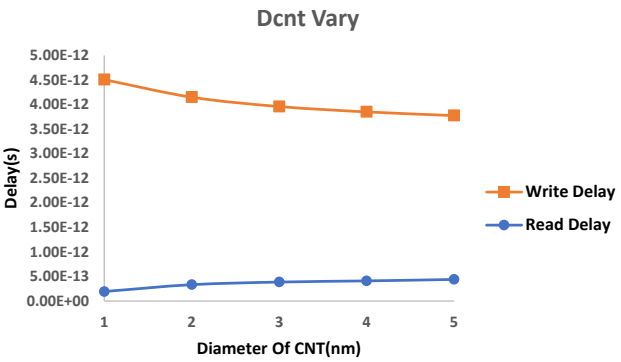

Fig 11: Write and read Delays of SRAM by varying the diameter of CNT.

Flat band voltage (Vfb) plays a crucial role in determining the threshold voltage and the performance of a CNTFET. A higher flat band voltage can result in a higher threshold voltage which can negatively impact the performance of the SRAM. Table 4 shows the read and write delays of SRAM with variable flat band voltage.

Table 4: Write and Read Delays of SRAM by varying the Flat band Voltage

Flatband Voltage(Vfb)	Write Delays(V)	Read Delay(V)
0v	4.29	0.43
0.04v	4.62	0.56
0.08v	4.95	0.63
0.12v	4.58	0.74
0.16v	5.64	1.17
0.20v	6.04	1.59

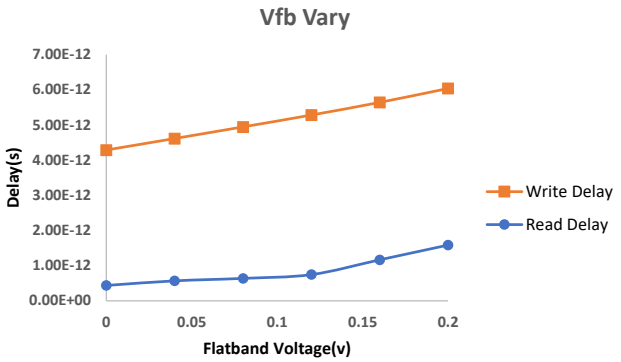

Fig 12: Write and Read Delays of SRAM by varying the Flat band Voltage.

In a CNTFET, the number of CNT tubes used in the device can also have significant impact on its electrical properties and performance. Table 5 is composed of the varying CNT tubes with decrease in read and write delays of SRAM. Analysing the figure 14 that we can conclude that 1V VDD has less read and write delays compared to the other voltage ranges.

Table 5: Write and Read delays of SRAM by varying the Number of CNT tubes

Number of CNT Tubes	Write Delays(ps)	Read Delay(ps)
1	5.43	0.613
2	5.36	0.610
3	5.35	0.598
4	5.35	0.594
5	5.35	0.591

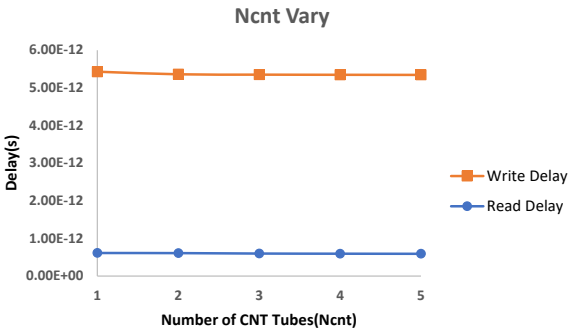

Fig 13: Write and Read delays of SRAM by varying the Number of CNT tubes.

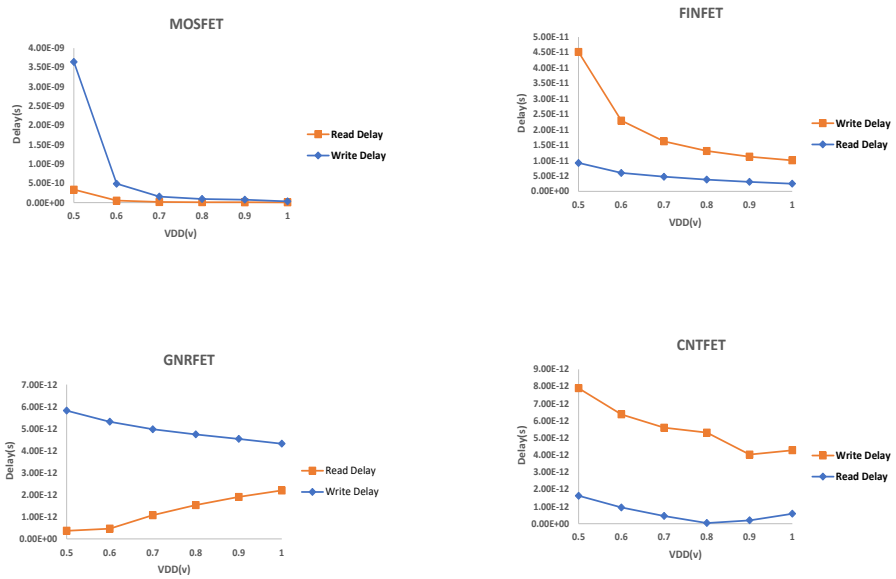

Fig 14: Read and write delays of SRAM by varying the VDD using Different FETs.

4 Conclusions

SRAM is the most used memory in many applications and it perform better way and have more stability than DRAM. In this work, we have analysed the performance of the 6T SRAM cell which is built by using the different field effect transistors. We have used the different field effect transistors such as FinFET, GNRFET and CNTFET to design a SRAM. All the SRAM design have compared with the conventional MOSFET designs. The comparison of simulation results have done at 32nm technology node which shows the delays, power dissipation, power delay product and static noise margin(SNM) is more marginal for CNTFET compared to other different FETs. Optimized CNTFET SRAM cell compared with the MOSFET based SRAM the write and read delays are improved by 85.8% and 94.3% respectively.

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