

Improving the quality indicators and performance of logical blocks and static memory of the microprocessor as part of improving the energy efficiency of devices

Vladimir Zolnikov^{1*}, Vyacheslav Reznichenko², Gleb Arakelyan², and Lyubov Manukhina³

¹ Voronezh State Forest Engineering University, 394087 Voronezh, Russia,

² Moscow Aviation Institute (National Research University), 125993 Moscow, Russia

³ Moscow State University of Civil Engineering, 129337 Moscow, Russia

Abstract. The study is aimed at consideration of improving the energy efficiency of devices. The article discusses methods for ensuring resistance to heavy charged particles (HCP) of a microprocessor RAM unit. A description of the implementation and a block diagram of static memory based on dummy blocks is provided. The work discusses methods of combating the bipolar effect, which are aimed at controlling the potential of the transistor body and reducing resistance. The dependence of the critical charge of a SOI memory cell on the gain of a parasitic bipolar transistor is modeled. To increase the fault tolerance of combinational circuits consisting of control logic and decoder blocks, redundancy is used at the level of individual gates. The article is considered to be useful for IT engineers and energy engineers, as well.

1 Introduction

To ensure resistance to special factors, as well as to maintain the correctness of the internal timing diagram of the RAM block, it is possible to design control logic using so-called dummy blocks [1-3].

In Fig. Figure 1 shows a possible implementation of a RAM block based on the proposed methodology. The circuit has a simple asynchronous interface, the timing diagram of which is shown in Fig. 2. The read cycle is initiated by any address change. The address decoder produces a clock pulse "atd", from which the sample enable signal "enb" is generated with a certain delay. A high-level impulse appears on the selected line "WL" and the row of cells we need opens.

In addition to the sampling signal, precharge shutdown pulses "pre" and read amplifier gates "sae" are also generated. The precharge must be disabled at the time when any array row is selected. In order to achieve an exact match between the "pre" and "WL" pulses in all three blocks, using the same control logic, the pre pulse generation circuit was assembled from elements borrowed from the decoder.

* Corresponding author: wkz@rambler.ru

In this case, it is possible to use read amplifiers based on a switchable pair of inverters connected to each other. After the "WL" signal is given, the cell begins to charge the bit lines, which causes an increase in the potential difference on the arms of the amplifier. When the "sae" signal is received, the inverters are energized and the read data is amplified to a complete logic difference.

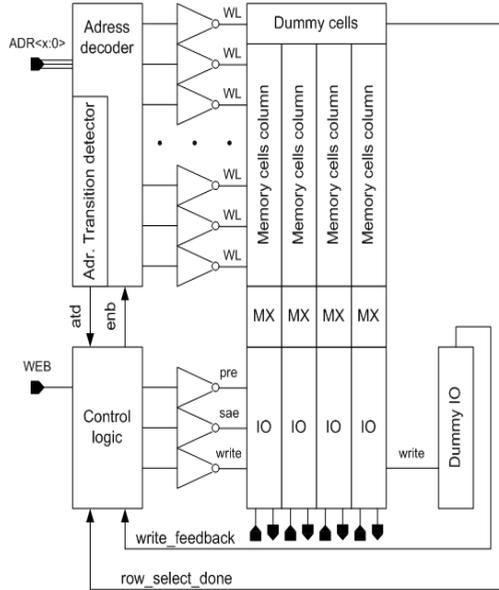


Fig. 1. Block diagram of a static RAM block

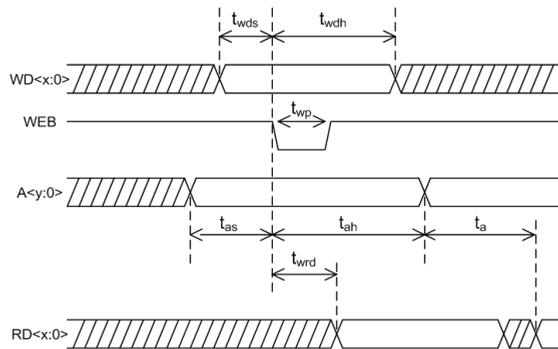


Fig. 2. RAM Time Diagram

In order to reliably read the correct data, the "sae" pulse must arrive after the row of memory cells is guaranteed to be selected. Initially, it was planned to form "sae" from the "enb" sample resolution signal, including an additional delay in the circuit. However, in the case of special factors, the required optimal delay changes, which can lead to incorrect operation of the unit as a whole. This can be avoided by entering an additional row of "Dummy cells" that have the same capacity on the "WL" input as the main memory cells, but do not participate in the storage of information. In the above scheme, the pulse "sae" is formed from the signal "row_select_done" that has already been delayed for the required time, which is the optimal solution in this case. The recording takes place on the negative edge "WEB", while the control logic (Control Logic) generates a "write" signal, for the state of which a latch is provided. To determine the required delay after which write will be disabled, an additional write buffer is introduced into the memory circuit, the output of which

is connected via the "write_feedback" line and a small latched delay. In this way, the duration of the "write" pulse will vary, thus keeping the write buffers running at the desired level.

Failure of decryptors can lead to access to the wrong memory address. During a write operation to an erroneously opened address, both the target write address and the erroneously opened address will be corrupted. During the read operation, if the decryptor fails, the wrong value will be read.

Structurally, the interpretation path consists of a combination scheme and powerful drivers of word sampling lines. If a charged particle hits the combination part of the circuit, it may fail and, as a result, be incorrectly selected. If a particle enters the driver area, it is highly likely that its effect will be negligible.

The protection of the combination part of the decoder circuit should be carried out in the same way as the protection of the control logic blocks.

2 Materials and methods

The main methods of dealing with the bipolar effect are to improve the control of the transistor body potential and reduce the source-body resistance. These methods make it possible to minimize the negative impact of the bipolar effect on the threshold failure rate and thus increase the failure tolerance of the protected devices [4, 5].

An equivalent scheme for simulating the ingress of a THD into a memory THD cell is shown in Fig. 3, and the simulated dependence of the critical charge of the memory THD cell on the gain of the parasitic bipolar transistor and on the grounding resistance of the transistor body in Fig. 4 [6].

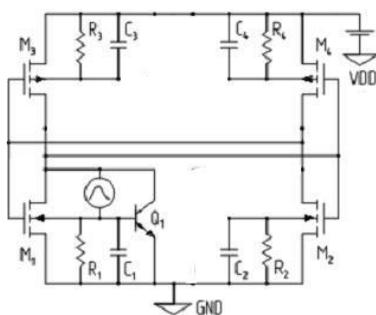


Fig. 3. Equivalent scheme for simulation of the ingress of TZP into the memory THD cell

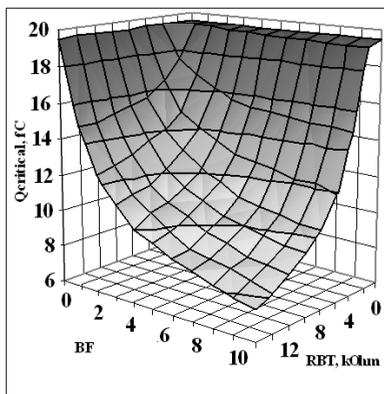


Fig. 4. Simulated dependence of the critical charge of the memory THD cell on the gain of a parasitic bipolar transistor and on the grounding resistance of the transistor body

Currently, a large number of variants of static memory cells with increased fault tolerance have been developed [7-9].

The first option that has emerged is to include resistors or RC circuits in the feedback circuit. A development of the idea of RC circuits is a memory cell with active RC circuits, shown in Fig. 5.

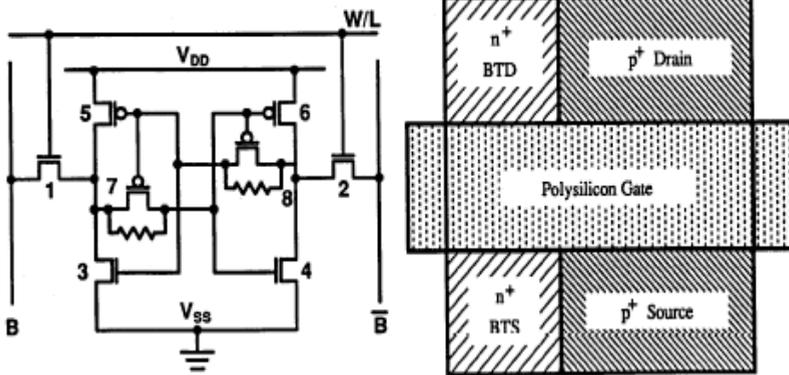


Fig. 5. Memory Cell, and Active RC Circuit Topology

The proposed active RC circuit is designed as a long-channel p-type transistor, in which the body is shorted at the same time as the drain and the source. When a supply voltage is applied to the gate of the transistor, there is no channel, and the effective resistance is equal to the relatively high resistance of the diffusion resistor formed by the transistor body. When there is ground on the transistor gate, the channel is open and the resistance drops dramatically. This design makes it possible to significantly increase the time constant of positive feedback without changing the charge resorption time, which makes it possible to increase the critical charge of the cell without large area losses.

A common option for protecting memory circuits is the DICE cell [10-13] (Dual Interlocked Cell), shown in Fig. 6. It consists of four inverters with cross-connected gates. Thus, each inverter is connected to the other two, which practically eliminates the failure as a result of the TZF getting into one of the transistors.

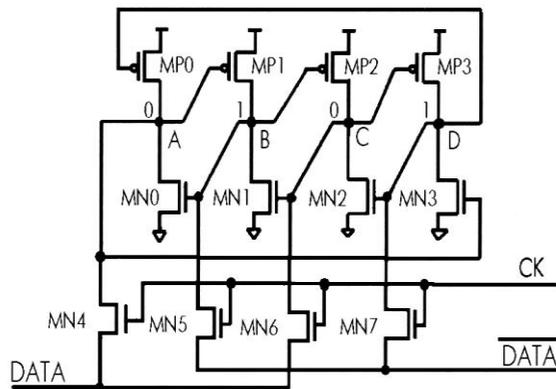


Fig. 6. ICE Memory Cell

With a high resistance to single failures, the DICE cell is very sensitive to simultaneous entry into two transistors, which becomes a significant problem when the design standards

are reduced to 250-180 nm. In this case, it is necessary to use special topological techniques for the geometric separation of the cell parts [10].

In the fault-tolerant IBM cell shown in Fig. 7, special circuits are applied, which are feedbacks that maintain the state of the cell during storage and are disabled by the write/read signal.

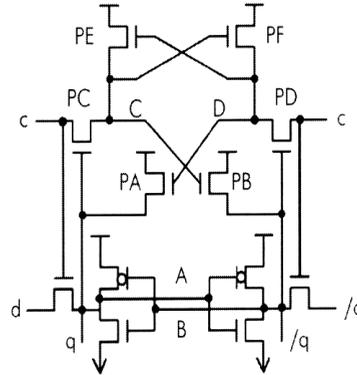


Fig. 7. IBM Fault-Tolerant Memory Cell

A fault-tolerant HIT (Heavy Ion Tolerant) cell is built on a similar principle to the IBM cell, but has a different structure, as shown in Fig. 8. Specifically, a storage cell consists of six transistors. This cell is used by Atmel for its microcontrollers, DSPs, and microprocessors.

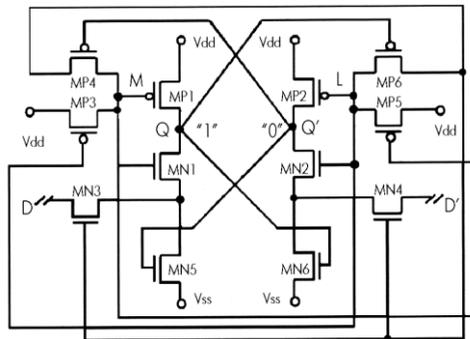


Fig. 8. HIT-Fault-Resistant Memory Cell

Over the years, the NASA (National AeroSpace Agency) has developed two fault-tolerant memory cells. NASA cell option 1, shown in Fig. 9, comprises two cross-connected four-transistor memory elements and four access transistors. Cross-control of the gates is applied in two cells, which avoids a failure when hitting any of the transistors.

In the NASA cell option 2, shown in Fig. 10, the memory elements are six-transistor, and each memory element has two pairs of feedbacks, one of which is controlled by the other memory element. Such a scheme is more reliable and stable than the earlier one. Both NASA cells are used in different versions of RAD (PowerPC Radiation-Resistant RISC Processors) processors.

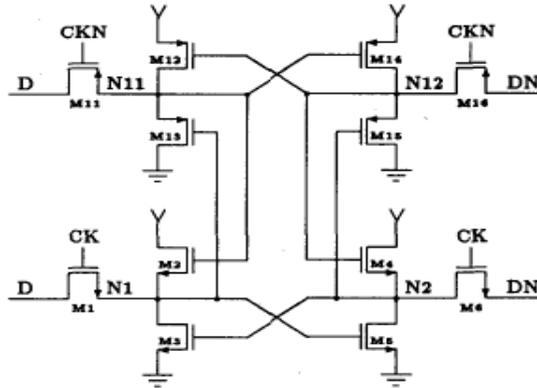


Fig. 9. NASA Memory Cell Option 1

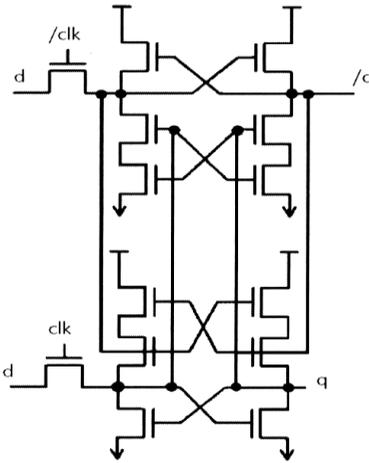


Fig. 10. NASA Memory Box Option 2

According to the literature, all of the above-mentioned variants of static memory cells have a high resistance to single failures, which makes it possible to compensate for two to three times the sensitive volume. Thus, according to the published experimental data, no failures were found in the cell studied by DICE at an LPE of more than 100 MeV/(mg/cm²). More recent studies on similar cells with lower design standards have revealed the need for additional protection against simultaneous damage to several transistors by a single particle.

3 Research and results

The control logic and memory decoder blocks are a combination scheme. Combination schemes typically consist of logic functions and ticked triggers that remember the result of the computation. The former are characterized by needle-type failures (DSET), while the latter are characterized by memory switching (SEU). Thus, the task of increasing fault tolerance is divided into two – separately for combination and sequential schemes.

Logic circuits are characterized by single transient type failures (DSET), which increase in importance as the operating frequency increases and the clock period decreases. Especially dangerous are failures in the clock circuits, which can lead to serious disruptions in the

operation of the device [11,14,15] In VLSIs with increased durability (such as microprocessors or systems-on-a-chip), the clock circuits are protected first [12, 16-18].

Increasing the fault tolerance of combination schemes can be realized by means of redundancy at the level of individual valves. Representatives of this class of circuits are the DDSL (Dual Data Stream Logic) and CVSL (Cascode Voltage Switch Logic) families, shown in Fig. 11. These schemes use data flow dualization to suppress failures in one of the channels. In DDSL, the signals on the two channels are identical in normal mode, while in CVSL they are opposite.

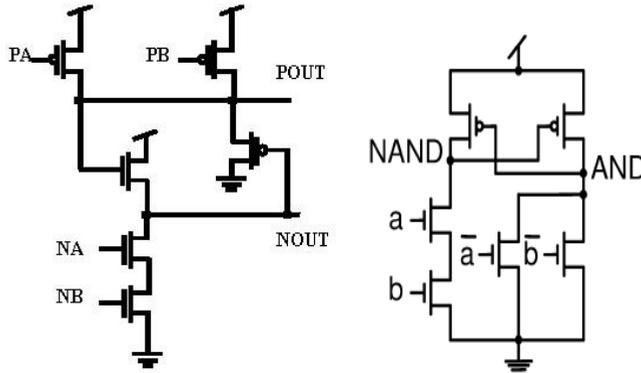


Fig. 11. 2I-HE logic element implemented in DDSL and CVSL

When a fault occurs in one of the channels, cross-feedback changes the voltage at the power transistor drain of the other channel, which in turn reduces the current flowing through the open transistor of the affected channel. Thus, with the help of feedbacks, the charge flowing through the circuit in the event of a failure is reduced and the failure threshold is increased.

Such schemes are slightly inferior to the standard CMOS in terms of functional parameters (about 10-30% in terms of area, speed and power consumption), while giving an increase in resistance to the through-passage of transients caused by the impact of single particles, which is shown in Fig. 12.

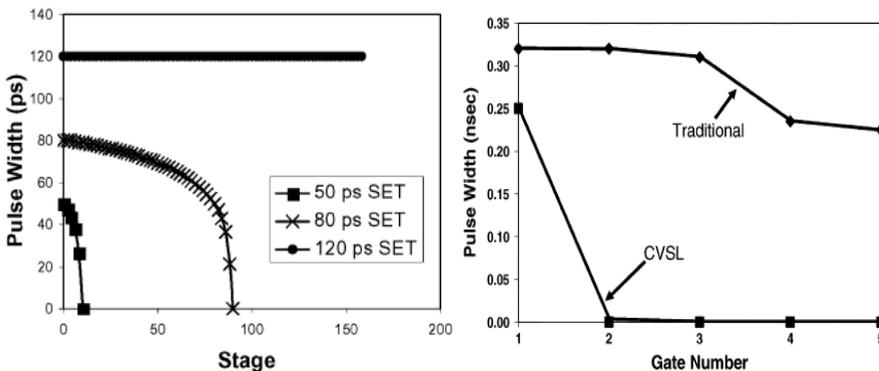


Fig. 12. End-to-end single failure (DSET) through a sequence of logic elements of traditional and CLSL logic

From Fig. As can be seen from Figure 13, the transient process is completely suppressed by passing through a chain of two or three CVSL gates, regardless of the pulse parameters, whereas in conventional circuits, relatively long transients can propagate over hundreds of valves in series, propagating through the circuit and causing severe disruptions. With this

feature in mind, an original method of redundancy using CVSL logic elements was proposed, shown in Fig. 13.

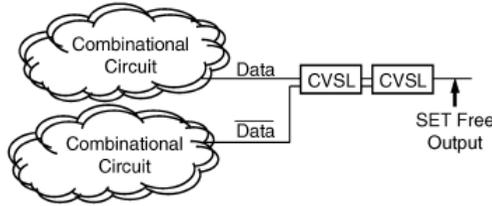


Fig. 13. Redundancy Based on CVS Logic

Serial circuits contain memory elements and control logic, resulting in two types of failures: memory switching (SEU) and control and clock failure (DSET). The presence of a bistable cell allows the use of circuitry solutions in triggers similar to those used in static memory circuits, such as RC circuits or DICE memory elements.

Since the reading amplifier is based on a bistable memory cell, the technique for increasing the durability of the amplifiers is somewhat similar to the technique for increasing the durability of memory cells.

The size of the transistors of the bistable cell is chosen to be large enough, and their optimal ratio is observed in order to ensure the equality of critical charges for the P- and N-types. It should be taken into account that increasing the size of the transistors increases the input capacitance of the amplifier. Thus, it may be necessary to increase the size of the feed-through switches, both at the input of the amplifier and in the column multiplexer. However, even in this case, the capacitance of the amplifier will be a small fraction of the capacitance of the bit lines, which has a mostly parasitic component [16-18].

The read amplifier can also be made according to the DICE circuitry, this applies to both the reinforcement cell and the receiving latch. This solution will avoid failures in the amplification and storage phases, but will increase the input capacity by about 2 times. Nevertheless, the charge accumulation phase will still remain susceptible to TZ, but, as mentioned above, its duration is short and is no more than 10% of the read cycle time. In real-world conditions, not every clock cycle occurs, the frequency may be less than the maximum possible for a given block, and the accumulation time may be reduced by means of programmatically configurable registers. In this way, it is possible to reduce the duration of the most sensitive phase to a value of the order of one percent.

In memory blocks that do not require high performance, it is acceptable to use a slower read amplifier circuit based on differential stages. Such a scheme contains only one asynchronous trigger, which stores the amplified data, the amplification itself is performed by a simple combination scheme. Despite the expected increased resistance to single failures, a differential cascade-based circuit may have dose problems [19-20].

4 Conclusion

Memory using one of the fault-tolerant cell variants requires a much larger area than standard memory using Hamming encoding, which can be more efficient with conventional memory cells and provided that a reliable and fast Hamming encoder/decoder is developed.

The main problems of implementing encoding in memory are the variable bit width of information, and the relatively low speed of the encoder/decoder.

The use of information of different bit sizes leads to the need to use an encoder of the minimum bit width used, which has a lower encoding efficiency, or to add zeros to the unused memory, reducing the available memory when using small bit widths of information.

A Hamming encoder/decoder (or other code designed to protect against failures) is a complex combination scheme that has a significant response delay, which can lead to an unacceptable increase in memory access time. In addition, the encoder itself can be prone to single failures, which can reduce the effectiveness of encoding.

References

1. V.K. Zolnikov, S.A. Evdokimova, T.V. Skvortsova, *Modelirovanie sistem i protsessov* **12**, 25-30 (2019)
2. K.A. Chubur, A.Y. Kulai, A.L. Savchenko, K.V. Zolnikov, A.E. Gridnev, *Modeling of Systems and Processes* **13**, 83-87 (2020)
3. I.I. Strukov, S.V. Grechanyi, A.S. Yagodkin, A.N. Chernikov, *Modeling of systems and processes* **13(2)**, 72-76 (2020)
4. V.K. Zolnikov, et.al, *Modeling of systems and processes* **13(3)**, 53-58 (2020)
5. V.K. Zolnikov, et.al, *Development of a test crystal in the design of CMOS microcircuits* **13(3)**, 58-65 (2020)
6. V.K. Zolnikov, et.al, *Modeling of systems and processes* **13(3)**, 71-76 (2020)
7. V.K. Zolnikov, et.al, *Verification of projects and creation of test sequences for microcircuit design* **12(1)**, 10-16 (2019)
8. E.V. Grosheva, et.al, *Modeling of Systems and Processes* **16(3)**, 30-41 (2023)
9. D.V. Shekhovtsev, et.al, *Modeling of systems and processes* **16(3)**, 79-86 (2023)
10. D.V. Shekhovtsev, et.al, *Route of design and testing of analogue blocks of the RTL model of the software and analytical complex of SAPR* **16(3)**, 86-93 (2023)
11. M.I. Kolesnikov, et.al, *Modeling of systems and processes* **16(1)**, 46-56 (2023)
12. F.V. Makarenko, et.al, *Application of negative logic elements in the construction of energy-efficient combination device* **16(1)**, 56-66 (2023).
13. A.V. Poluektov, F.V. Makarenko, R.Yu. Medvedev **16(1)**, 77-84 (2023)
14. A.V. Poluektov, R.Yu. Medvedev, V.K. Zolnikov, *Modeling of systems and processes* **16(1)**, 106-115 (2023)
15. V.K. Zolnikov, et.al, *Modeling of processes in semiconductor structures under radiation impact* **15(4)**, 106-115 (2022)
16. Y. Deniskin, *E3S Web of Conferences* **164** (2020)
<https://doi.org/10.1051/e3sconf/202016410042>
17. A.V. Tolkachev, *Modeling and management of the chaotic process* **15(4)**, 128-136 (2022)
18. D. Yurin, et.al, *E3S Web of Conferences* **244** (2021)
<https://doi.org/10.1051/e3sconf/202124411010>
19. A. Korchagin, et.al, *Transportation Research Procedia* **63**, 1521-1533 (2022)
<https://doi.org/10.1016/j.trpro.2022.06.164>
20. A.S. Yagodkin, et.al, *Development of algorithms and programs for the analysis of electrical characteristics of LSI* **15(4)**, 136-148 (2022)