

# Fault Mitigation in Seven-Level Diode Clamped with Static Switch Based Fourth Leg Inverter Topology for Induction Motor Drives

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**Abstract:** Modern day life demands the use of inverters at the point of utilization for many of the applications especially for motor drives used in industrial applications. Conventional inverters suffer from a setback of high harmonics at the output of inverter. Multi-level inverters produce stepped output nearer to sinusoidal reducing the harmonic distortion at the output. Faults are quite common in occurrence in inverters and needs to be identified and mitigated as quickly as possible. This paper presents seven-level diode clamped multi-level inverter topology with fourth leg for fault mitigation. Fourth leg is operated with thyristor based control and gets activated from the signals obtained from algorithm. An algorithm was given to identify the fault and send activating signals to fourth leg of inverter. Fault was internally generated only in phase-A in inverter circuits which can be applied the effectiveness of four-leg topology to phase-B and phase-C of inverter as like in phase-A. Simulation work was carried out and results were obtained using MATLAB/SIMULINK software.

**Keywords:** Diode Clamped Multi level inverter, open fault, mitigation, algorithm, induction motor drive.

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## 1. Introduction

Motor drives a part of industries these days. For almost every application in industries, motors are needed. AC and DC motors are the type of motors. DC motors having brushes and commutator produces sparks creating additional losses. This makes a way for AC motors to be used in industries and also synchronous motors in AC type need additional start-up methods to start them. Induction motor which is simple and robust and simple in construction having fine speed regulation is widely used motor in industries [1-4]. Speed control of motors is needed to fit a particular application and thus needing a speed control circuit. Motor with speed control system is called motor drive system.

Variable speed obtained from variable frequency method in induction motors is efficient method to control speed of induction motor [5-12]. To obtain a variable frequency to drive induction motor, inverter is a good option. Use of inverter driven induction motors are increasing day by day. A conventional inverter produces output containing large disturbances due to presence of harmonics. This harmonics might affect the motor performance. Presence of harmonics demand additional bulky filters to smoothen the output of inverter for satisfactory performance of motor drive which in turn increases the overall system cost. Multi-level inverters can be a good solution to this problem producing a nearer sinusoidal output in stepped-form containing low harmonic distortions. Faults are more in occurrence in inverter circuits and need to be identified and mitigated as soon as possible [13-14]. Almost 70% of faults are open type of faults and the same fault condition was considered in this paper for the mitigation.

A seven-level diode clamped inverter topology was considered in this paper for induction motor drive. A four-leg topology of diode clamped inverter was developed over conventional diode clamped inverter for fault mitigation. Fourth leg was driven by a thyristor based circuit to which activating signals were obtained from an algorithm for fault identification and mitigation. This algorithm identifies the fault (open type of fault considered in this paper) and if fault is identified, immediately algorithm sends activating signal to the thyristor circuit, this thyristor circuit stimulates the fourth-leg of diode clamped inverter. When fault was identified, fourth leg replaces the faulty phase and the diode clamped inverter operates under normal operation as if no fault

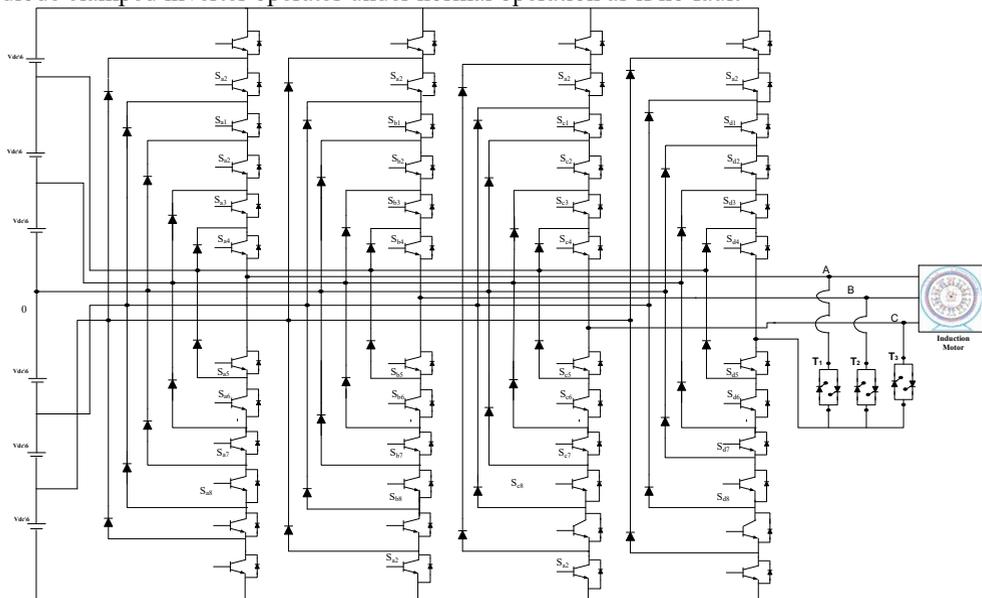


Fig. 1: Seven-level four-leg Inverter with induction motor.

## 2. Multi-level four-leg topology

The power industry has shown a great interest in multi-level inverters recently, primarily due to the growing demand for power. Unlike conventional two-level converters that provide a two-level output matching the input DC bus voltage, multi-level inverters offer stepped output levels that resemble a sinusoidal waveform. This increase in levels helps to reduce total harmonic distortion. Additionally, multi-level inverters allow for the adjustment of voltage and frequency.

The diode clamped multi-level inverter utilizes clamping devices, with diodes serving as these devices. The configuration proposed, depicted in Figure 1, is a seven-level four-leg inverter that incorporates an additional fourth leg to a conventional three-leg inverter. This fourth leg becomes operational when a fault is detected in the inverter circuit. Thyristors are responsible for its operation, as they send triggering signals to the power electronic switches in leg-4. By deactivating the switches in the faulty phase, the faulty leg is disconnected from the circuit. Simultaneously, the fourth leg inverter controlled by thyristors, it can acts as an active leg to replace the faulty one. As previously mentioned, the fourth leg is governed by thyristors, and the algorithm sends active signals to these thyristors, which then activate the corresponding switches in leg-4 to function actively in place of the faulty phase. The algorithm that triggers the respective thyristors is elaborated in the subsequent section.

## 3. Algorithm for fault mitigation

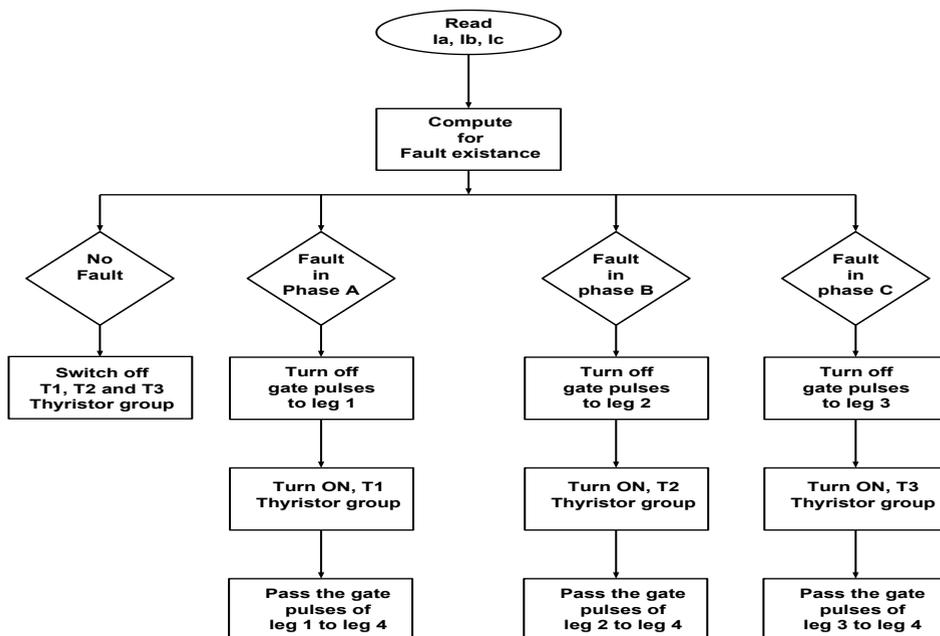


Fig .2: Fault mitigation algorithm.

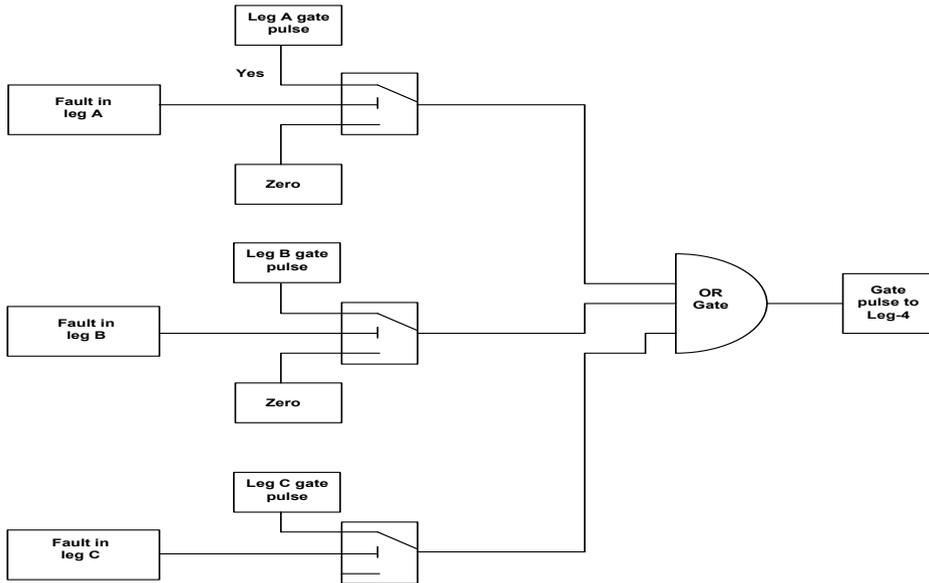


Fig .3: internal algorithm for activating fourth leg.

In fault mitigating algorithm shown in fig. 2 initially, phase currents in individual phases at the output of induction motor were sensed. As the current in open circuit will be zero, the read phase currents were sent to compute their values to identify whether the read phase currents are non-zero values with amplitude or zero value. The computation of fault existence plays a crucial role in the algorithm. If the computed value detects the presence of a fault, the signal will be transmitted to the corresponding steps. Additionally, in the absence of any faults, the command will be issued to deactivate thyristor groups  $T_1$ ,  $T_2$ , and  $T_3$ . In the event that the computed value detects a fault in phase A, a command will be sent to deactivate the gate pulses to phase A. Subsequently, thyristor group  $T_1$  will be activated, bypassing the gate pulses from leg 1 to leg 4. Similarly, if a fault is detected in phase B, a command will be sent to deactivate the gate pulses to phase B. Then, thyristor group  $T_2$  will be activated, bypassing the gate pulses from leg 2 to leg 4. Likewise, if a fault is detected in phase C, a command will be sent to deactivate the gate pulses to phase C. Subsequently, thyristor group  $T_3$  will be activated, bypassing the gate pulses from leg 3 to leg 4. The internal algorithm for bypassing arbitrary faulty phase gate pulses to leg 4 was shown in fig. 4. If fault exists in phase A, the selection switch receives signal and sends active signal to OR gate. Similarly if fault exists in phase B, the selection switch receives signal and sends active signal to OR gate and the same for phase-C like if fault exists in phase C, the selection switch receives signal and sends active signal to OR gate. The OR gate sends command to activate leg 4 and thus mitigating the fault. For bypassing gate pulses from faulty phase to fourth phase, an internal algorithm to activate fourth leg was given in fig. 3.

#### 4. Seven-level four-leg topology with fault mitigating algorithm

Figure 4 illustrates a diode clamped inverter fed induction motor drive with four legs and seven levels. The fault existence in the diode clamped inverter is determined by sensing and computing the output phase currents. Gate pulses are produced for the four legs of the inverter in accordance with the fault mitigation algorithm. In the event of a fault in the inverter circuit, the gate pulses to the faulty phase semiconductor switches are turned OFF, disconnecting the faulty phase from the main circuit. The gate signals are then

redirected to the fourth leg, allowing the inverter to operate normally as if no fault had occurred.

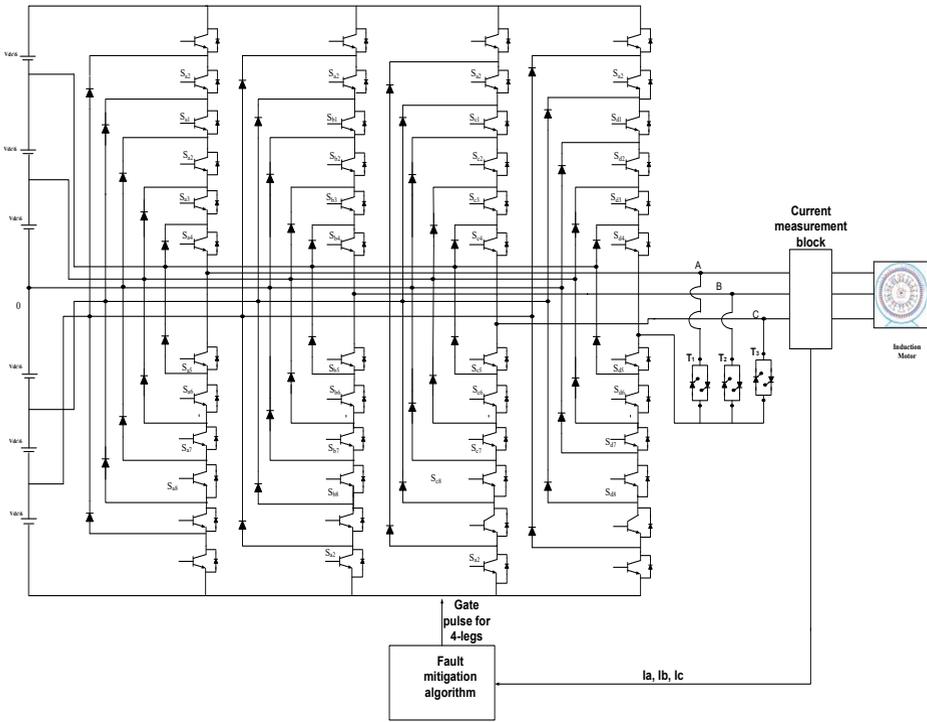


Fig .4: Proposed model with fault mitigation.

### 5. MATLAB results and illustrations

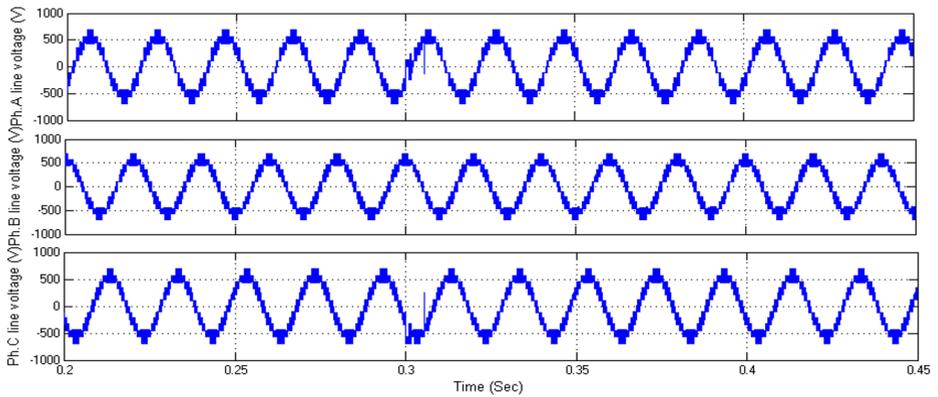


Fig .5: Line voltages in seven-level four-leg inverter fed drive under fault mitigation.

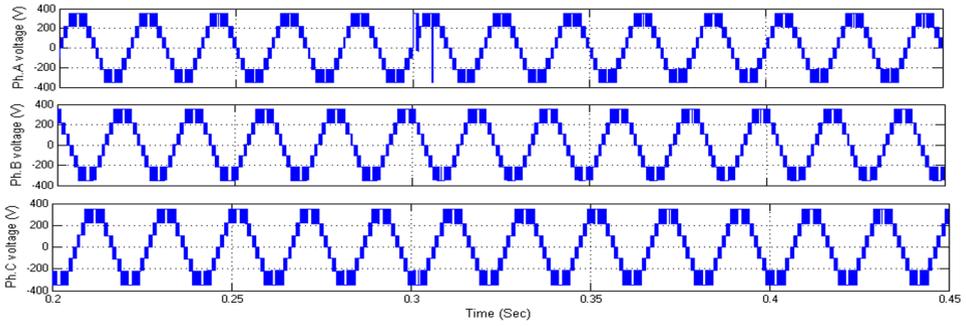


Fig .6: Phase voltages in seven-level four-leg inverter fed motor under fault mitigation.

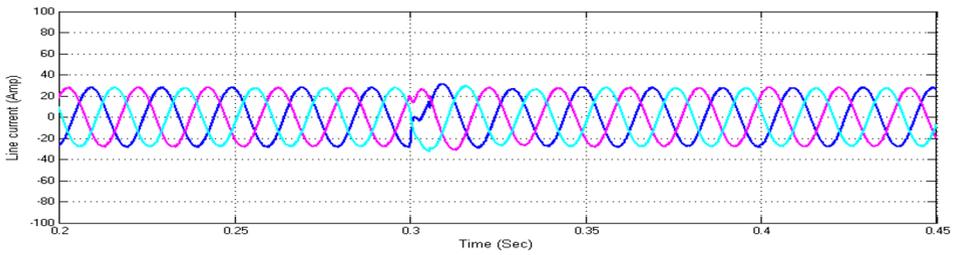


Fig .7: Line currents in seven-level four-leg inverter fed motor under fault mitigation.

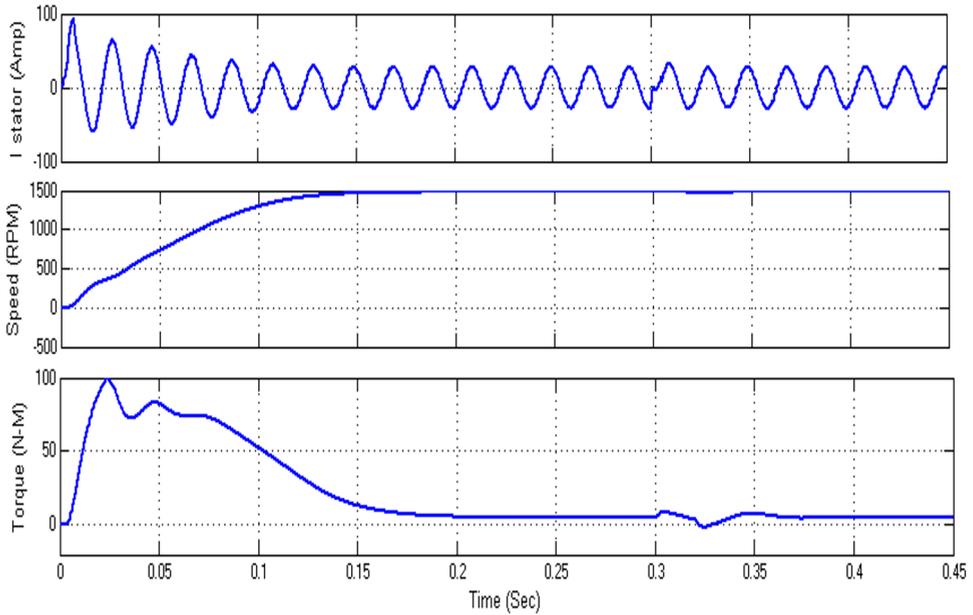


Fig .8: Stator current, speed and torque under fault mitigation.

Figures 5 and 6 depict the line voltages and phase voltages of a proposed seven-level four-leg diode clamped inverter fed induction motor with fault mitigation. Figure 7 showcases the line currents of the induction motor drive. Furthermore, figure 8 presents the

induction motor characteristics, including stator current, speed, and torque. At 0.3 seconds, a fault was detected, but thanks to the activation of the fourth leg of the diode clamped inverter, the fault was promptly resolved. Consequently, the fault was successfully mitigated, and the induction motor characteristics returned to their normal state without any disruption in the performance of the induction motor drive and phase voltage, even after the fault was identified.

## 6. Conclusions

Multi-level inverters proved to be very effective solution delivering quality output with less harmonic distortions as compared to conventional inverter. Multi-level inverter fed induction motor drives are becoming familiar these days. Faults are occurs very often and needs to be mitigated in inverter fed drives. This paper presents seven-level diode clamped inverter with four-leg topology for mitigation of faults in inverter. Fault mitigation algorithm was explained which drives thyristors connected to fourth leg operation. Whenever thyristor circuit is active, drives fourth leg and mitigates the fault by excluding faulty phase. Motor characteristics were shown where no disturbances in performance curves are observed. Algorithm works satisfactorily in clearing the faults of inverters.

## References

- [1] A. A. Ansari and D. M. Deshpande, "Induction Motor Efficiency Optimization Using Fuzzy Logic," *International Journal of Advanced Engineering and Applications*, Vol. 1, 2010, pp. 177-180.
- [2] C. Thanga Raj, S. P. Srivastava, and Pramod Agarwal, , "Energy Efficient Control of Three-Phase Induction Motor - A Review," *International Journal of Computer and Electrical Engineering*, Vol. 1, No. 1, April 2009, pp 1793-8198.
- [3] H. Sarhan and R. Issa, "Modeling, Simulation and Test of Inverter-Induction Motor Drive System with Improved Performance," *Journal of Engineering Sciences*, Assiuit University, Vol. 33, No. 5, 2005, pp. 1873-1890.
- [4] Hussein Sarhan "Energy Efficient Control of Three-Phase Induction Motor Drive," *Energy and Power Engineering*, 2011, pp 107-112.
- [5] E. Najafi and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4148-4154, Nov. 2012.
- [6] J. A. Ferreira, "The multilevel modular DC converter", *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460-4465, Oct. 2013.
- [7] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [8] Paavo Rasilo, Aboubakr Salem, Ahmed Abdallah, Frederik De Belie, Luc Dupré and Jan A. Melkebeek, "Effect of Multilevel Inverter Supply on Core Losses in Magnetic Materials and Electrical Machines", *Energy Conversion IEEE Transactions on*, vol. 30, pp. 736-744, 2015.
- [9] Nakul Thombre, Ratika singh Rawat, Priyanka Rana, Umashankar S, "A Novel Topology of Multilevel Inverter with Reduced Number of Switches and DC Sources", *International Journal of Power Electronics and Drive System (IJPEDS)*, Vol. 5, No. 1, pp. 56~62, July 2014.
- [10] S. Mekhilef, "Digital control of three phase three-stage hybrid multilevel inverter", *IEEE Trans. Ind. Electron.*, vol. 9, no. 2, pp. 719-727, May 2013.
- [11] H. W. Ping, N. A. Rahim and J. Jamaludin, "New three-phase multilevel inverter with shared power switches", *J. Power Electron.*, vol. 13, pp. 787-797, 2013.
- [12] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEE Transactions On Industrial Electronics*, Vol. 49, No. 4, pp. 724-738, August 2002
- [13] F. W. Fuchs, "Some diagnosis methods for voltage source inverters in variable speed drives with induction machines—A survey," in *Proc. IEEE Ind. Electron. Conf.*, 2003, pp. 1378–1385.

- [14] D. Diallo, M. E. H. Benbouzid, D. Hamad, and X.Pierre, "Fault detection and diagnosis in an induction machine drive: a pattern recognition approach based on concordia stator mean current vector," *IEEE Trans. Energy Conv.*, vol. 20, no. 3, pp. 512-519, Sept. 2005.