A New Symmetrical Cascaded Single Phase H Bridge Inverter With Reduced Switch Count

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***Abstract*—An imaginative multilevel inverter topology is presented with the intent of deploy few series connected switches, ameliorate modularity and derogatory voltage stress collate to unremarkable topologies which is published in literature [1] and [2]. This paper mainly focuses on symmetrical configuration. Modified sinusoidal pulse width modulation (MSPWM) technique is developed in this paper with less number of carrier requirement compared to traditional sinusoidal pulse width modulation. This generalized structure and MSPWM technique will give the advantage of less cost of device, compact size.**

***Keywords*—CHBMLI, Multilevel Inverter, MLI, PWM.**

1. INTRODUCTION

Inverter is a contrivance which permutes fixed DC to variable AC. Inverter is categorized into two types, one is Current Source Inverter (CSI) and other one is Voltage Source Inverter (VSI). CSI requires more filter requirement compared to VSI drives it is due to more distortions are present in output of the CSI. Hence for medium and high power applications VSI is better choice in terms of less components and better performance than CSI. VSI can be classified into two types.

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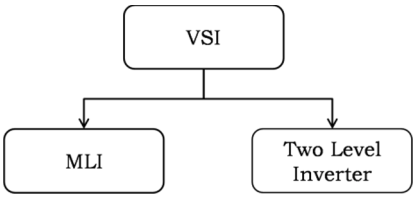

Fig. 1. Classification of VSI.

Classic two level inverter provides $+V_{dc}/2$ and $-V_{dc}/2$ at the output. Although this method of generating AC is easy but it introduces more distortions in the output and it also have high voltage stress compared to that of MLI. MLI is a forward step of a two level inverter. It is not possible to get smooth stepped output waveform from a two level inverter, more than two voltage levels are required to generate smooth waveform with low distortions. The fancy of multilevel power conversion is to conglomerate stepped waveform from several sources to procure an output voltage nearer to sinusoidal in lineament and have the eminence of steer at higher power and higher voltages with meager series connected switches, deteriorated voltage stress and ameliorate modularity. In practice MLIs are deficient to beneath levels, in view of the fact that it's increased switch count at higher levels. This intensification in switch count not only swivel the topology ticklishness but also raises its overall cost. From past couple of decades, there is an exceptional scrutiny carried out to blossom newer topologies with narrow switch count. Some of its radical applications comprehend industrial drives, FACTS devices, electric vehicles and renewable energy sources. Frequently used MLI topologies are namely cascading H-bridge inverters (CHBMLI), MLI with clamping diodes and flying capacitors. These are shown in Fig.2.

DCMLI and FCMLI uses single DC link sources where as CHBMLI uses multiple DC link sources. In DCMLI when number of stages increasing then DCMLI requires excess clamping diodes and control of real power flow is difficult. The control of real power flow can be achieved by FCMLI but it also requires auxiliary capacitors for voltage balance. The disadvantages of both inverters are overcome by using CHBMLI. CHBMLI has some features like modularity in structure, easy to control, simple in design, reliable and no voltage balancing problems.

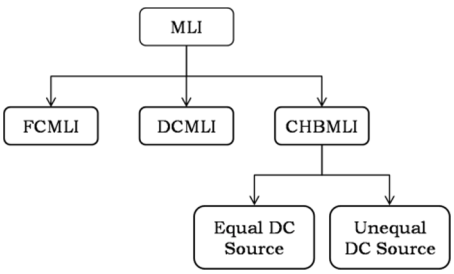

Fig.2 Classification of MLI.

Multi levels can be generated by adding number of CHB basic units in series. Hence the structure says modularity that is basic units can be connect or disconnect without disturbing other basic units.CHB is again classified into two types one is symmetrical CHB and another one is asymmetrical CHB.

In symmetrical CHB the magnitude of all voltage sources are identical where as in asymmetrical configuration the voltage sources are not identical. This paper develops a new generalized symmetrical configuration with fewer numbers of switches. The entire work is validating through MTLAB/SIMULINK software.

2. PROPOSED TOPOLOGY

The proposed topology has four sources and four switches.

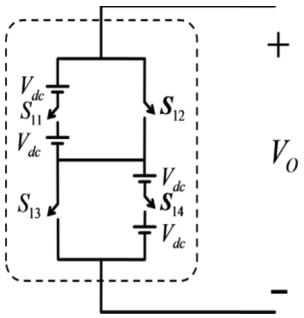

Fig.3 Proposed Basic Unit.

When S_{12} and S_{13} is ON the output voltage is 0.When S_{11} and S_{13} is ON the output voltage is $2V_{dc.}$When S_{11} and S_{14} is ON the output voltage is $4V_{dc}$. The remaining voltages levels V_{dc} and $3V_{dc}$ cannot be obtained from this basic unit to get remaining voltage levels an auxiliary circuit is connected in series with basic unit. The auxiliary circuit consist two switches S_A and S_B along with a source. The basic unit without auxiliary circuit is obvious in Fig.3.

TABLE I. DIFFERENT LEVELS OF PROPOSED BASIC UNIT

Switch status				Output voltage
S_{11}	S_{12}	S_{13}	S_{14}	
0	1	1	0	0
1	0	1	0	$2V_{dc}$
1	0	0	1	$4V_{dc}$

The auxiliary unit with basic unit is shown in the following Fig.4 and corresponding voltage levels are mentioned in Table 2.

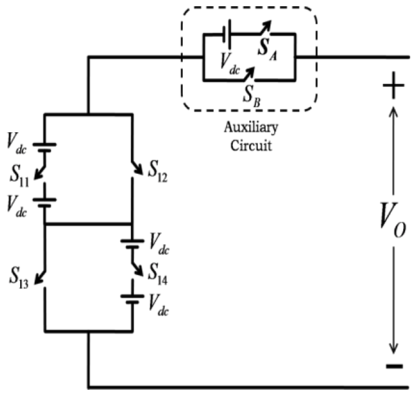

Fig.4 Proposed Basic Unit with an Auxiliary Circuit.

TABLE II. DIFFERENT LEVELS OF PROPOSED BASIC UNIT WITH AN AUXILIARY CIRCUIT

Switch status						Output voltage
S_{11}	S_{12}	S_{13}	S_{14}	S_A	S_B	
0	0	0	0	0	0	0
0	1	1	0	1	0	V_{dc}
1	0	1	0	0	1	$2V_{dc}$
1	0	1	0	1	0	$3V_{dc}$
1	0	0	1	0	0	$4V_{dc}$
1	0	0	1	0	1	$5V_{dc}$

The maximum output voltage obtained from this basic unit is $5V_{dc}$. The voltage values are positive since the current direction is same throughout the basic unit. Hence the output waveform is consist only positive levels to obtain complete cycle another cascade H-bridge is connected in parallel with basic unit along with an auxiliary circuit. The corresponding framework is obvious in Fig.5.

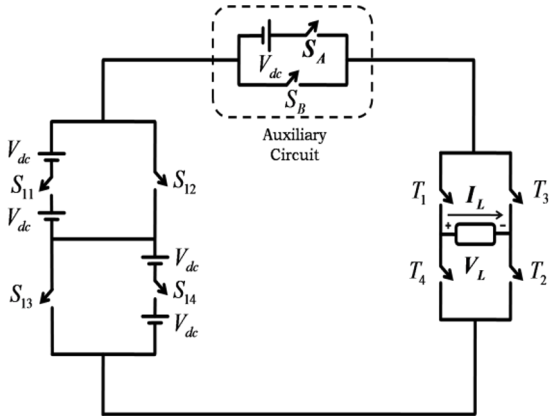

Fig.5 proposed multilevel structure with single basic unit.

Proposed MLI structure can give rise to both positive and negative levels. When switches T_1 and T_2 are switched ON the output levels are in positive direction. The output levels are in negative direction when switches T_3 and T_4 ON. Number of series connected 'n' number of basic units will give m levels.

Finally essential number of Switches "N_{switch}" and number of DC sources "N_{source}" in CHBMLI's to generate "m" levels in voltage are approved by the relevant equations respectively.

$$N_{Switch} = \left(\frac{m-3}{2}\right) + 6 \tag{1}$$

$$N_{Source} = \frac{(m-1)}{2} \tag{2}$$

Where "m" = number of output levels.

3. COMPARING THE PROPOSED TOPOLOGY WITH CONVENTIONAL TOPOLOGIES

Conventional topologies are published in literature from [1] –[8].The nominated topology need few series connected switches collate to those existing topologies hence it is better in terms of derogatory switching losses and conducting losses. The conventional and proposed topologies are obvious in below Fig.6.

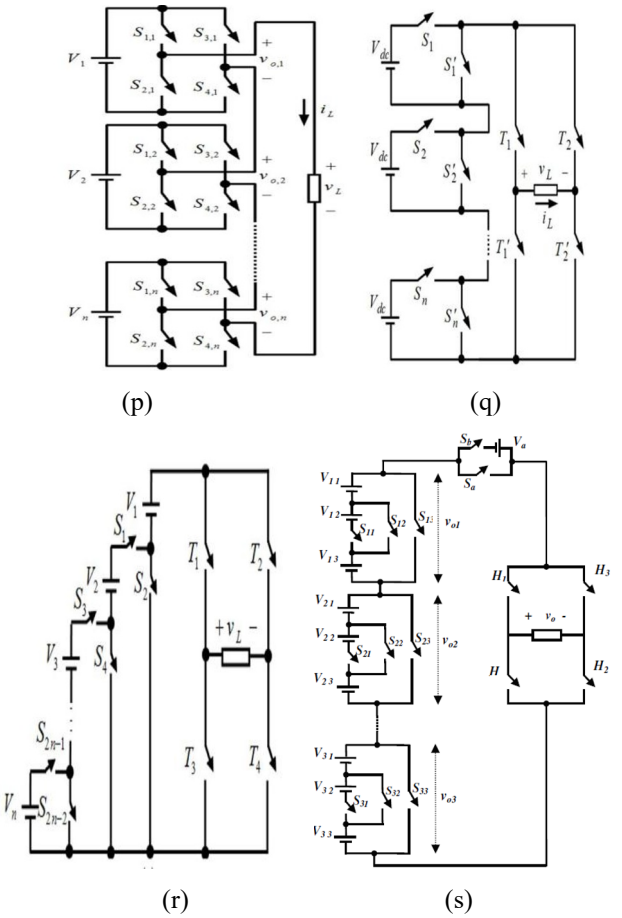

Fig.6. Different MLI Topologies, (p). Described in [2], (q). Described in [3], (r). Described in [4], (s). Described in [5].

TABLE III. CORRELATION FACTORS OF CONVENTIONAL AND PROPOSED TOPOLOGY

Parameter	**[2]**	**[3]**	**[4]**	**[5]**	**Proposed Topology**
Number of Switches	2(m-1)	(m-1)	(m-3)	(m+1)	$\left(\frac{m-3}{2}\right)+6$

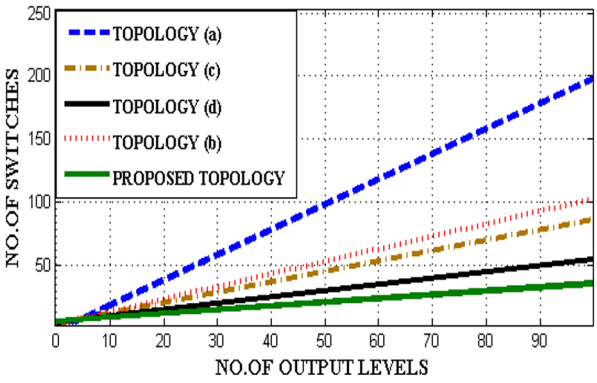

Fig.6 Number of Levels vs Number of Switches.

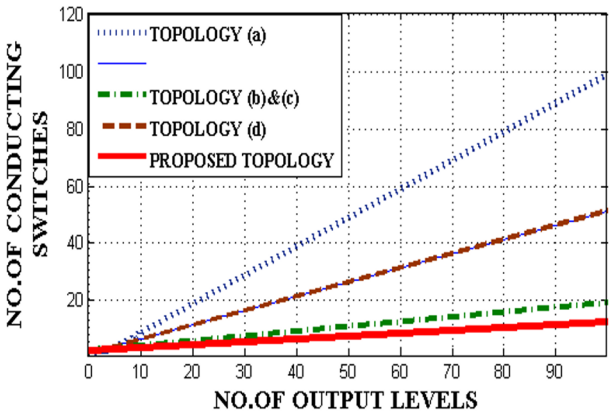

Fig.7 Number of Levels vs Number of Conducting Switches.

4. MULTILEVEL MODULATION TECHNIQUES

Power dissipation of switches like diode, transistors and thyristors mainly depends on switching frequency. Hence switching frequency plays key role in controlling of the VSI inverters. There are different types switching frequency pwm techniques these are mentioned in below Fig.8.

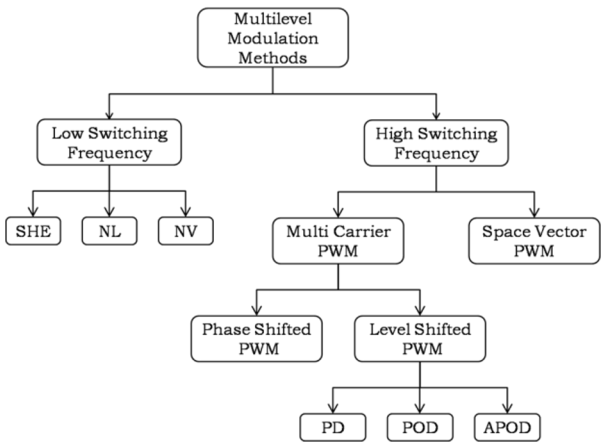

Fig.8 Multilevel Modulation Techniques.

High switching frequency modulation technique has better performance in terms of lower output distortion, faster load response, and compact size of the equipment. This paper focus on lower output distortion and less size of the equipment hence high switching frequency modulation method is best choice for this proposed topology.

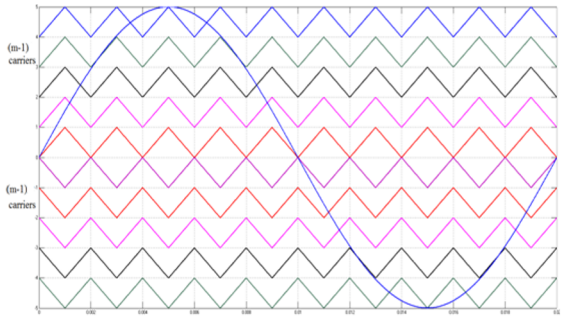

Fig.9 Conventional PDPWM for 11-Level Inverter.

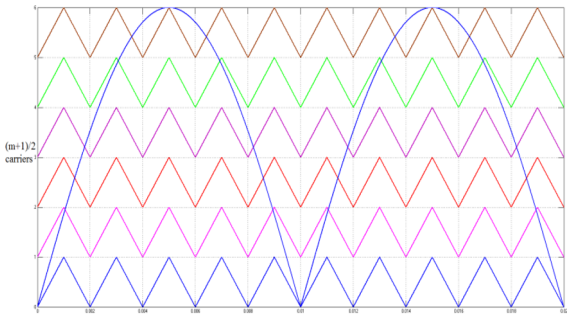

Fig.10 Modified PDPWM for 11-Level Inverter.

High switching frequency modulation methods are again classified into two types one is SVPWM and another one is multicarrier PWM. When number of levels are going to increase SVPWM technique complexity is increase. For simplicity of designing of topology for m number of levels multicarrier PWM is alternate choice .Conventional PWM uses (m-1) number of carriers for generating AC hence it is named as multicarrier PWM technique. It further categorized as phase shifted PWM (PSPWM) and level shifted PWM (LSPWM).In PSPWM carriers are arranged in horizontal manner where as in LSPWM carriers are lay out in vertical manner. The vertical arrangement of carrier dominance to low distorted line voltage at the output compared to PSPWM. LSPWM additionally categorized into phase disposition (PD), phase opp0sition and disp0sition (POD) and alternate phase opposition and disp0sition (APOD). A modified phase disposition PWM technique is preowned in this paper which requires (m+1)/2 carriers. For example if m=11 which indicates the number of levels conventional PDPWM requires 10 carriers on the other hand modified PDPWM (MPDPWM) requires 6 carriers almost half of the carriers will be reduce in case of MPDPWM. The corresponding diagrams are shown in Fig.9 and Fig.10 respectively.

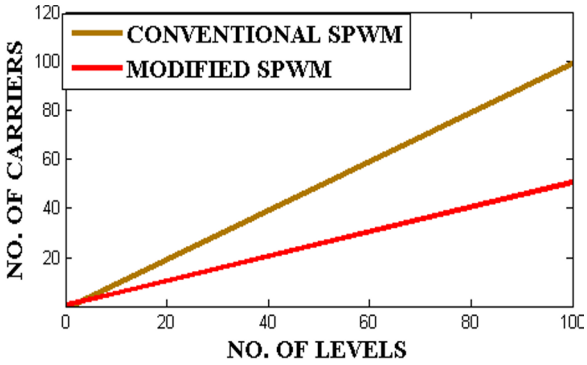

Fig.11 Number 0f Levels Vs Number of Carriers.

Fig.11 shows carrier comparison between conventional SPWM and modified SPWM

5. SIMULATION RESULTS

In this section all the work is done by employing MATLAB/SIMULINK software. The specification parameters of nominated topology is listed in Table 4.The results are shown for 2 basic units with different modulation index values and the output voltage value and %THD for 3 basic units.

TABLE IV. SPECIFICATION PARAMETERS OF PROPOSED TOPOLOGY

Parameter	Value
Input voltage	20V
Fundamental frequency	50Hz
Carrier frequency	50kHz
Resistance	10Ω

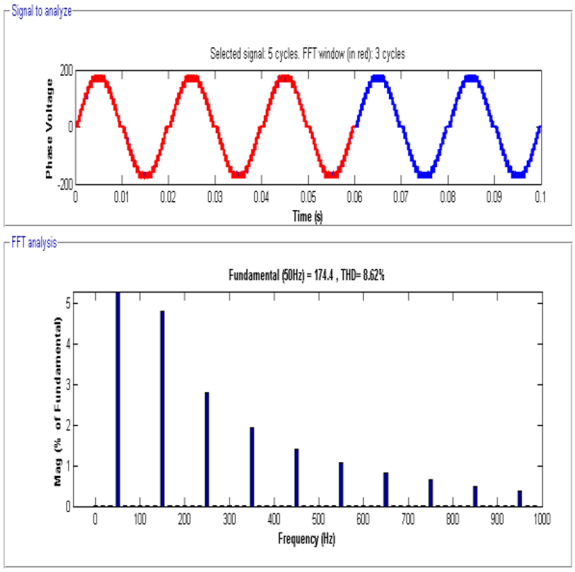

Fig.12 Proposed Topology 0utput Voltage and %THD if m_a=1.

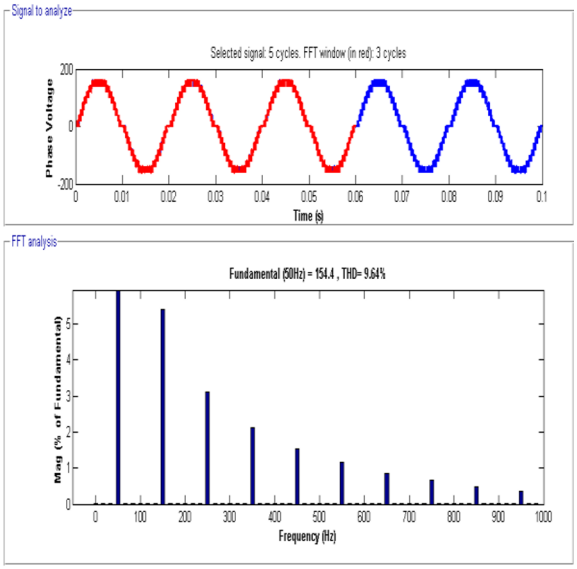

Fig.13 Proposed Topology 0utput Voltage and %THD if m_a=0.9.

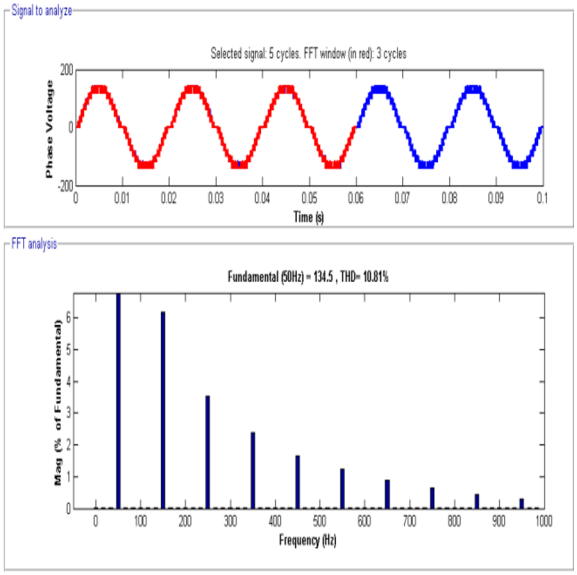

Fig.14 Proposed Topology 0utput Voltage and %THD if m_a=0.8.

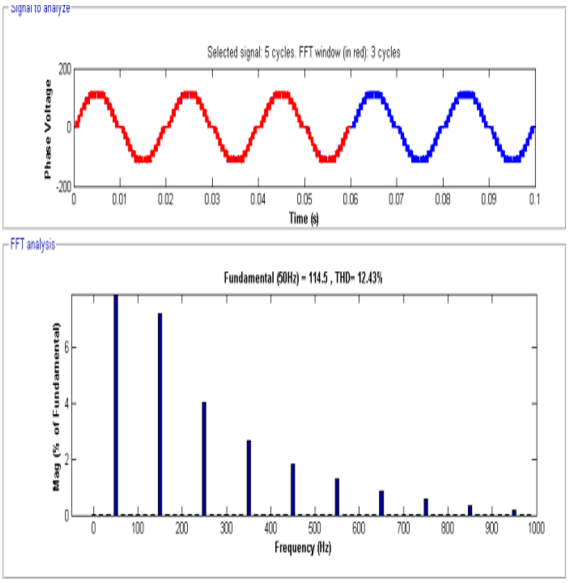

Fig.15 Proposed Topology 0utput Voltage and %THD if m_a=0.7.

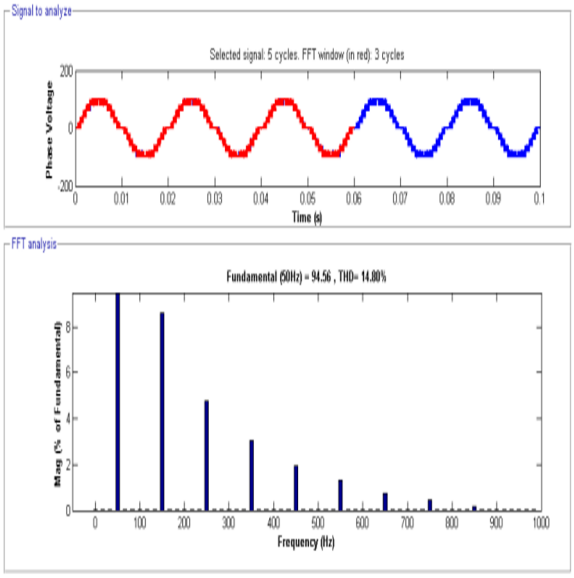

Fig.16 Proposed Topology 0utput Voltage and %THD if m_a =0.6.

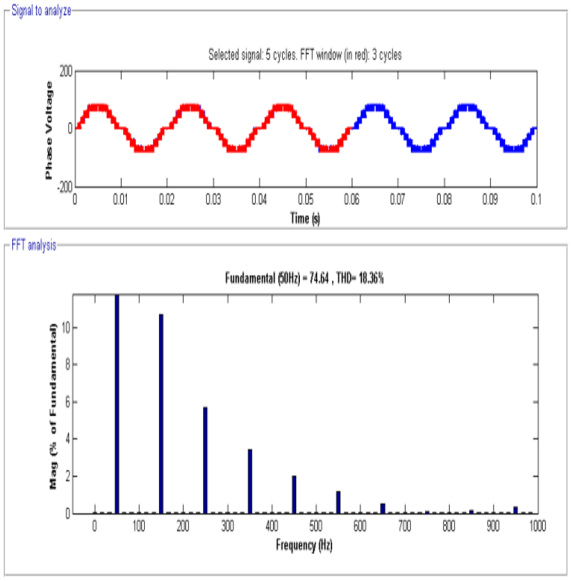

Fig.17 Proposed Topology Output Voltage AND %THD for m_a=0.5.

TABLE V. OUTPUT VOLTAGES AND %THD OF PROPOSED TOPOLOGY

S.No	m_a	Output Voltage	%THD
1	1	174.4 V	8.62
2	0.9	154.4 V	9.64
3	0.8	134.5 V	10.81
4	0.7	114.5 V	12.43
5	0.6	94.56 V	14.90
6	0.5	74.64 V	18.36

6. CONCLUSION

A imaginative symmetrical H-bridge inverter is nominated and it is compared with existing topologies. This new topology (proposed topology3) will require less number of switches for "m" level output .The number of levels are extended by admix fundamental units in series. In nominated MLI, conducting Switches at higher output level requires less number compare to traditional topologies. Due to which conduction and switching losses are minimized.

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