

A Novel Seven Level Inverter with Reduced Switch Count and THD for PV System Applications

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Abstract:Based on economic, controllability and total harmonic distortion (THD) Multilevel inverters are more rising devices in many applications compare to other traditional inverters. Hence here a novel multilevel inverter (MLI) is designed and analysed with less count of switches and diodes. Generally (L-1) switches are required for conventional L level inverters like flying capacitor, diode clamped, and cascaded multilevel inverters but here a H-bridge inverter with additional two legs having less no of switches is introduced. The converter's controllability plays a crucial role in enhancing the THD of the output voltage and efficiency. Here a level shifted sinusoidal pulse width modulation technique is implemented i.e Phase Opposition Disposition SPWM (PODSPWM) method, because of it gives better THD over other level shifted SPWM techniques like PDSPWM, APODSPWM, COSPWM, VFSPWM and Phase shift SPWM techniques. The Design and analysis of this seven level inverter is evaluated with the tool of MATLAB/SIMULINK.

Keywords: Multilevel inverter, SPWM Methods, THD.

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1. INTRODUCTION

The best way to use solar photovoltaic energy is using an inverter. To synchronise with the electrical grid, the inverter's output should have a higher voltage level. The output voltage of a two-level inverter looks like a classic, fundamentally square wave, which is a downside. A multilevel inverter overcomes the shortcomings of a two-level inverter. [1]-[2]

Multilevel inverters are preferred in situations demanding high power and medium voltage. Because power development is straightforward and common mode voltage, power losses, and dv/dt can all be reduced, it is possible to incorporate unconventional energy sources, high voltage DC transmission systems, flexible AC power transmission networks, and high-power motors. They are mentioned in [3] through [4]. Common topologies include those listed below. Among these are the diode-clamped, also known as the flying-capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge (CHB) multilevel inverters. The difficulty of regulating capacitor voltages increases significantly multilevel inverters has many output voltage levels. Numerous capacitors and diodes were required for the FC and NPC inverters, respectively. Numerous switches and isolated DC power supply are necessary for the modular CHB inverters [5]-[7].

Due to its ability to provide output voltages with exceptionally low distortion that are almost sinusoidal and operate at a reduced switching frequency, multilevel inverters are becoming more and more common in the industry. Numerous studies use space vector pulse width modulation techniques, third harmonics injection sinusoidal PWM methods, and other sinusoidal PWM methodologies [8]. They also produce less Common-Mode (CM) voltage, which lessens the strain on the motor bearings [9]. With the use of dynamic voltage balancing circuits and transformer-free semiconductor switches, an unique seven level inverter can achieve high voltage and high power. The harmonics produce Electromagnetic Interference (EMI), voltage, and current as the number of output levels rises [10]-[13]. The sinusoidal PWM procedure is adopted to create the triggering signals for the multilevel inverter, which was mentioned in [14]. To produce a low waveform distortion and almost sinusoidal output voltage, a triggering signal is necessary to operate each power semiconductor switch of the inverter. A new topology was invented in [15] with fewer components, however it offers high output voltage and current THD values. According to the research mentioned above, it is crucial to reduce the power component and improve the THD of output waveforms. In order to achieve this, a new design for a seven-level inverter is suggested here, with lower component count and a multicarrier Sinusoidal pulse width modulation approach for control.

2. CIRCUIT CONFIGURATION

2.1. Discription of operation of conventional 7-level diode clamped inverter

The conventional L-level Multilevel inverter consist by $2(L-1)$ switches and $(L-1)(L-2)$ Diodes for the L-level inverter. Hence for 7-level inverter consist by 12 main switches and 30 diodes which is shown in Fig.1

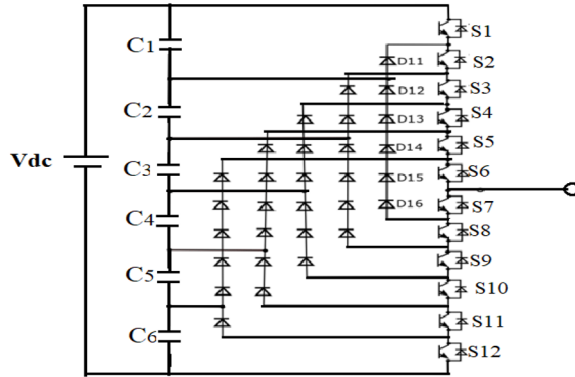


Fig.1. Conventional 7-level Diode clamped Inverter

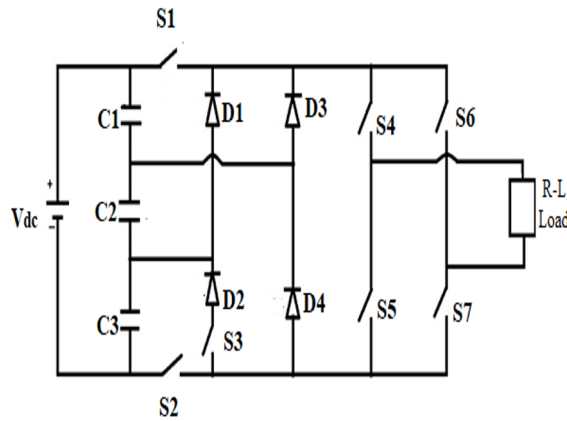


Fig.2. Proposed 7-level Inverter

2.2. Description of switching states for the proposed 7-level inverter

The input voltage in the proposed seven-level inverter is divided by the three series capacitors C1, C2, and C3, with each capacitor having a voltage of $V_{dc}/3$ across it. Through the employment of four diodes and three MOSFETs, the H-bridge, which consists of four MOSFETs, carries the divided voltage to the output terminal. Upon correct installation of the gate signal, the multilevel inverter as proposed has the capability to generate an AC output voltage consisting of seven levels. Table 1 displays the switching states of the proposed 7-level inverter.

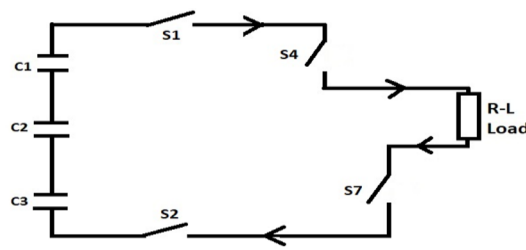
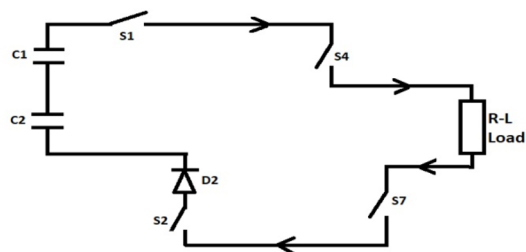
Table.1. various switching states of inverter.

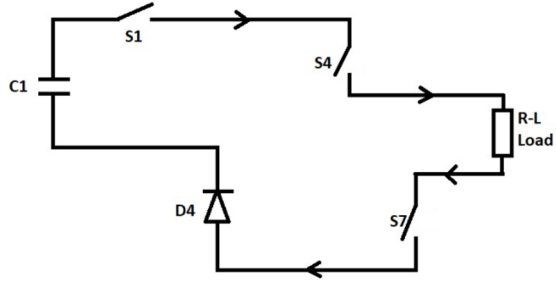
<i>Output Voltages</i>	<i>S1</i>	<i>S2</i>	<i>S3</i>	<i>S4</i>	<i>S5</i>	<i>S6</i>	<i>S7</i>
0	0	0	0	1	0	1	0
+Vdc	1	1	0	1	0	0	1
+2Vdc/3	1	0	1	1	0	0	0
+Vdc/3	1	0	0	1	0	0	0
-Vdc/3	0	1	0	0	1	1	0
-2Vdc/3	0	1	0	0	1	1	0

$-V_{dc}$	1	1	0	0	1	1	0
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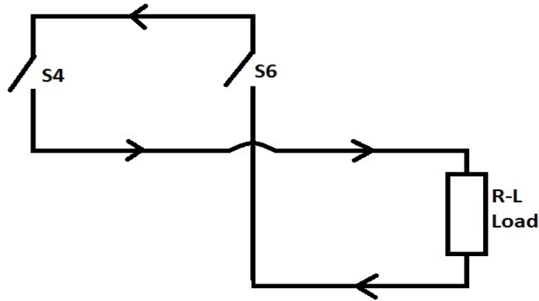
The following steps are taken to produce the needed seven voltage output levels of V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0 , $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$.

- S1 and S2 are activated to produce the voltage level $V_o = +V_{dc}$. The capacitors C1, C2, and C3 supply power. V_{dc} is the voltage across the H-bridge. S4 and S7 are switched ON, and V_{dc} is appear at the load terminals according to Fig.3.(i)
- S1 and S3 are activated to create the voltage level $V_o = +2V_{dc}/3$. The capacitors C1 and C2 supply power. There is a $+2V_{dc}/3$ voltage across the H-bridge. Amount of voltage sent to the load terminals is $+2V_{dc}/3$, and In accordance with Fig.3.(ii). S4 and S7 are both set ON.
- S1 is activated at the positive half cycle to generate a voltage of $V_o = +V_{dc}/3$. The H-bridge is powered by the capacitor C1, and there is a $V_{dc}/3$ voltage across it. S4 and S7 are switched ON, and $+V_{dc}/3$ is appear at the load terminals according to Fig.3.(iii)
- S4 and S6 are activated to create the voltage level $V_o = 0$. i.e at load terminals, no voltage is being applied according to Fig.3.(iv)
- S2 is activated while the negative half cycle $V_o = -V_{dc}/3$ voltage can appear across the load. The H-bridge is powered by the capacitor C3, and there is a $-V_{dc}/3$ voltage applied to it. The loading stations receiving a $-V_{dc}/3$ voltage when S5 and S6 are turned ON according to Fig.3.(v)
- By enabling S2, a voltage level of $V_o = -2V_{dc}/3$ is produced. The capacitors C2 and C3 supply power.
- There is a $2/3V_{dc}$ voltage across the H-bridge. In
- operation, S5 and S6 apply a $-2V_{dc}/3$ voltage to the load terminals as seen in Fig.3.(vi)
- The voltage achieved by turning ON S1 and S2 is $V_o = -V_{dc}$. Energy is provided by capacities C1, C2, and C3, and a voltage of $-V_{dc}$ powers the H-bridge. When S5 and S6 are turned on, the load terminals get a $-V_{dc}$ voltage, as illustrated in figure 3.(vii), which is shown in Figure 3.

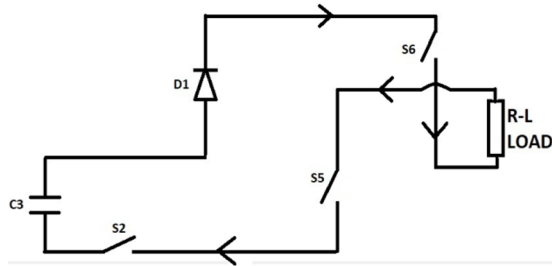
(i) $+V_{dc}$ level(ii) $+2V_{dc}/3$ level



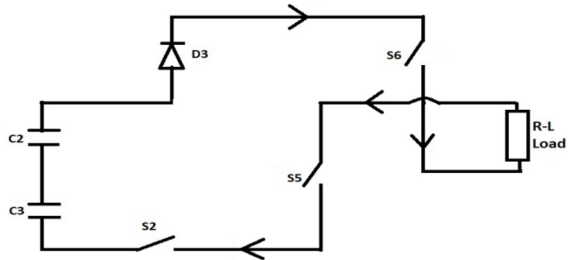
(iii) $+V_{dc}/3$ level



(iv) 0 level



(v) $-V_{dc}/3$ level



(vi) $-2V_{dc}/3$ level

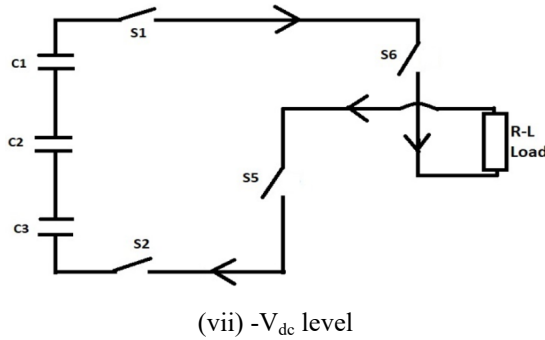


Fig.3. Switching states for various levels of proposed 7 level inverter

3. CONTROL TECHNIQUE

The majority of MLI are currently regulated using a variety of control approaches, including (I) space vector PWM, (II) phase shift PWM, and (III) level shift PWM. The inverter pulses are generated by comparing the carrier signals and sinusoidal waves in level shift control methods. These are again classed as PDSPWM, APODSPWM, PODSPWM, COSPWM and VFSPWM based on the locations of the carrier signals. All control methods exhibit carrier signals with a high frequency. For example, to produce a N level output voltage and current waveform, 1 reference signal with a frequency of 50 Hz is compared to 6 carrier signals of 2KHZ frequency. If reference signal (V_m) > carrier signal (V_c) for above reference axis and Reference signal (V_m) < carrier signal (V_c) for below reference axis are the conditions that cause the pulse to be produced. PODSPWM approaches, which are depicted in Fig.4., is used in all of the aforementioned SPWM techniques because they provided a better output voltage THD than other SPWM techniques, which may be discussed in the results.

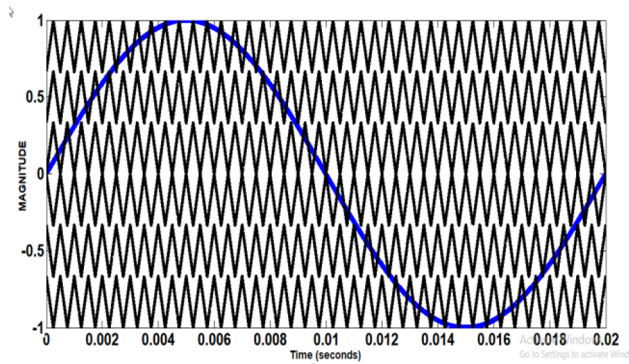


Fig.4.PODSPWM control technique.

4. RESULT AND DISCUSSION

Table.2. parameters.

S.NO	Parameter	Value
1	DC Voltage	240 V
2	Output Voltage	240 V

3	Output Current	4.6A
4	Dc link Capacitor	3e-3
5	Switching frequency	50 Hz
6	Carrier frequency	2000 Hz
7	Modulation Index	1
8	Load Resistance	50 Ohms
9	Load Inductance	35e-3 H

MATLAB/Simulink is applied to design and analyse the operation of the novel multilevel inverter which contain of seven-switches and four diodes only. Under normal operating conditions, the voltage of 7-level appears across R-L load, based on the switching pattern of the inverter is displayed in table.1. Consequently, the output voltage having seven levels, such as E_{dc} , $2E_{dc}/3$, $E_{dc}/3$, 0 , $-E_{dc}/3$, $2E_{dc}/3$, $-E_{dc}$, of magnitude of 240V is shown in Fig.5. This output has less THD i.e 9.94% compare to the conventional 7-level inverter and THD of ref [15]. In [15], which contain 8 switches with 4 diodes, and the THD of output voltage is 14.21% only. Here the circuit of [15] is modified with 7 switches and four diodes. Hence THD of output voltage is reduced which is displayed in Fig.7. The current through the R-L Load is shown in Fig.6, having magnitude of 5.8A and its THD analysis is also shown in Fig.8. This has less value i.e 3.68%.

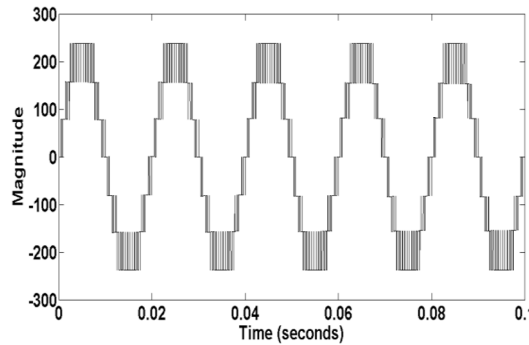


Fig.5 Output Voltage of proposed seven level inverter atMI=1.

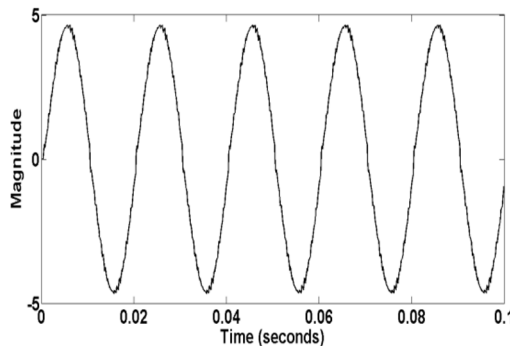


Fig.6. Output Current of proposed 7-level inverter

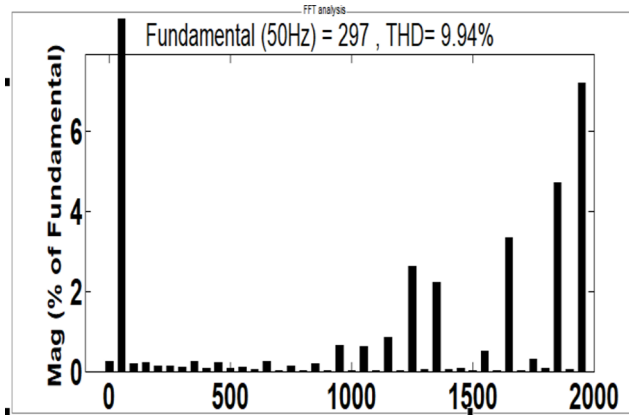


Fig.7. THD of 7-level Voltage.

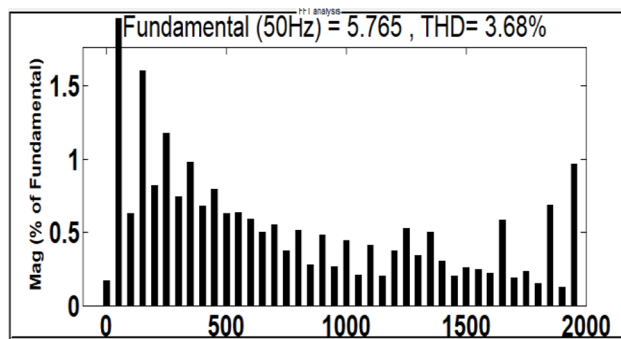


Fig.8 THD of 7-level Current.

This topology has to operate a 7-level inverter with better THD from 0.7 to 1.0 value of Modulation index. The same topology can be operates as 5-level inverter with reduced magnitude of 156 V from 0.4 to 0.6 of MI and act as a 3-level inverter with very less magnitude of 78 V from 0.1 to 0.3 of MI values these variations are shown in table.3. Therefore, it can be seen from this table that this inverter can work at various levels with various voltages. These 5-level and 3-level voltages with reduced magnitude are shown Fig.9. and Fig. 11 along with its Harmonic spectrums shown in Fig.10 and Fig 12. Table 3 and Figure 13 illustrate the THD of the output voltage across different Modulation index values.

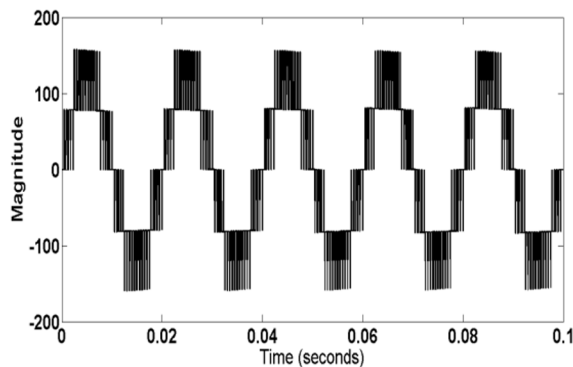


Fig.9. 5-Level output voltage at MI=0.5

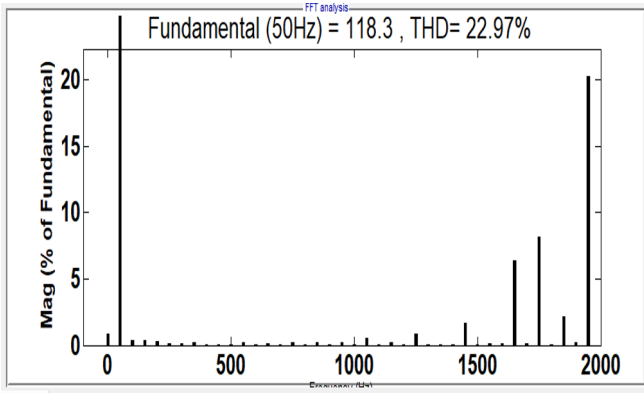


Fig.10.Harmonic spectrum of 5-level output Voltage

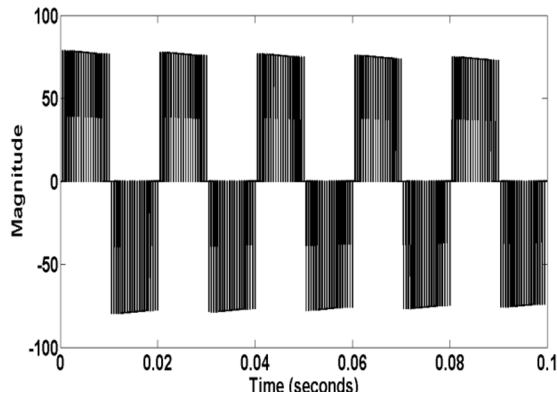


Fig.11. 3-Level output voltage at MI=0.3

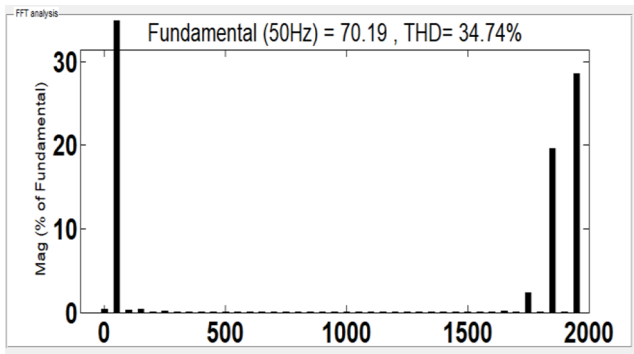


Fig.12. Harmonic spectrum of 3-level output Voltage

Table.3. Comparison of THD at various MIs

<i>Modulation Index</i>	<i>% THD</i>
0.1	89.5(3-L)
0.2	62.0(3-L)
0.3	34.74(3-L)
0.4	22.81(3-L)
0.5	22..97(5-L)
0.6	18.50(5-L)
0.7	13.41(7-L)
0.8	13.59(7-L)
0.9	12.91(7-L)
1	9.9(7-L)

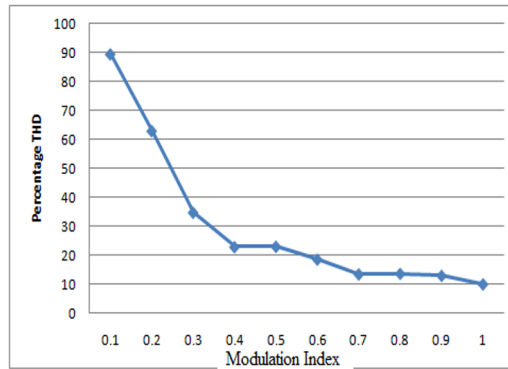


Fig.13. Comparison of THD at various MI values

Table.4. Comparison of THD for various topologies

<i>Topology</i>	<i>% THD (At Unity of MI)</i>
Conventional Inverter	21.63
Ref[15]	14.21
Proposed Inverter	9.94

5. CONCLUSION

The new 7-level inverter topology proposed in this research uses fewer switches and diodes than the conventional multilevel inverter. The modulation index plays an important key role in operating of the inverters, hence here it can be operated at various modulation index values and observed it can operate as a 7-level inverter, 5-level inverter and 3-level inverter at various MI values. The controllability is implemented by multicarrier PODSPWM technique to provide pulses to the inverter. The inverter costs less and has

better THD of output voltage and current compared to a conventional multilevel inverter since it has fewer switches and diodes. The effectiveness of the inverter is demonstrated by a simulation carried out in the MATLAB/Simulink environment.

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