A Novel Seven Level Inverterwith Modified Modulation Technique for Drive Applications

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ABSTRACT- For high-power, high-voltage applications, multilevel inverters have gained widespread acceptance. Due to its rising advantages. In this paper a new circuit multilevel inverter, comparatively speaking to traditional inverters, this design requires less components as well as fewer gate drives and carrier signals. Because of this, both the total expense and complexity are drastically decreased, especially for higher output voltage levels. This circuit consists by two components one is level generation part contain by four switches and other one is polarity generation part comprise by H-bridge inverter that make up output voltage as a seven level. The portion that generates levels employs high frequency switches to produce various levels, and the part that generates the polarity of the output voltage is at line frequency. Additionally, it is more effective due to an inverter component that uses line frequency to operate switching power devices. As a result, there is no requirement for all switches to operate at high frequency, resulting in easier and more dependable management of the inverter. Here multicarrier Phase Disposition Sinusoidal Pulse Width Modulation (PDSPWM) technique regulates the operation of the inverter.It consists by three carrier signals instead of six carrier signal and it provide less THD of output voltage and current compare to other multicarrier sinusoidal pulse width modulation techniques. The design, analysis and control of the seven level inverter is demonstrated with the help of MATLAB/Simulink tool.

Keywords: Multilevel inverters, Sinusoidal Pulse width Modulation, Total harmonic

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1. INTRODUCTION

The output voltage of a standard two-level inverter's is a quasi-square wave, and in order for the inverter to be connected to the electrical system, the output voltage has to be close to a sinusoidal wave. As a result, the filters needed for a two-level inverter are large and take up more space. Additionally, the inverter's voltage magnitude should be large enough as to synchronize with the grid; as a result, the system requires more powerful power electronic switches, which raises the cost and adds losses to the system. Multilevel inverters also gained a great deal of interest as power converters in various applications, including high-voltage DC transmission systems (HVDC), flexible AC power transmission systems (FACTS), the integration of renewable energy sources and big motor drives, due to their advantages over traditional two-level inverters.

Multilevel inverters were then developed and gained popularity as a result of its many benefits, including better THD, less switching losses, low voltage stress on switches and the elimination of the filter circuits, which reduces electromagnetic interference (EMI) [1]-[3].

The main idea behind the multilevel inverter is to use a larger quantity of active semiconductor switches to generate electricity in low voltage steps by expanding the number of output voltage levels.

Multilevel inverters offer output-voltage waveforms that are almost sinusoidal, output current with an excellent harmonic profile, a smaller filter, and less electromagnetic interference (EMI). They are lightweight and small in design attributable to all of these features [4]– [5].

Multilevel inverters can be configured in three different topologies: diode-clamped called as neutral point clamped (NPC) multilevel inverter [6]-[7], flying-capacitor (FC) multilevel inverter [8]-[9] and cascaded H-bridge (CHB) multilevel inverter [10]-[12].

The dimensions of passive output filters could be limited by using multilevel inverters, which may result in a decrease in system costs by reducing the voltage stress on power semiconductors [13]. Because of these advantages, multilevel topologies have recently gained attention as a potential application in PV systems [14]-[16]. Numerous diodes and capacitors were needed for the NPC and FC inverters, respectively. For the modular CHB inverters, numerous switches and a separate DC power supply are necessary [17].

However, expanding the levels of the voltage in multilevel inverters would result in a greater need for voltage sources, power switches and capacitors, which will significantly increase the inverter's cost and size. Additionally, addingmore switches will result in a complex control algorithm and problems with voltage imbalance.

Hence in this paper a novel topology which contains less no of main switches, diodes and capacitors compare to other conventional multilevel inverts which referred in above

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2. CIRCUIT OPERATION

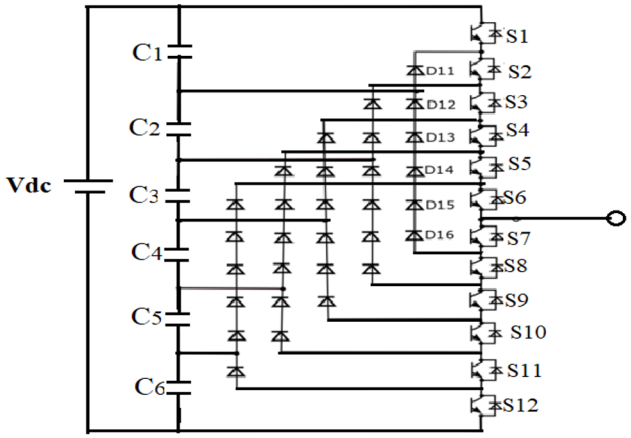


Fig.1. Conventional 7-level diode clamped inverter

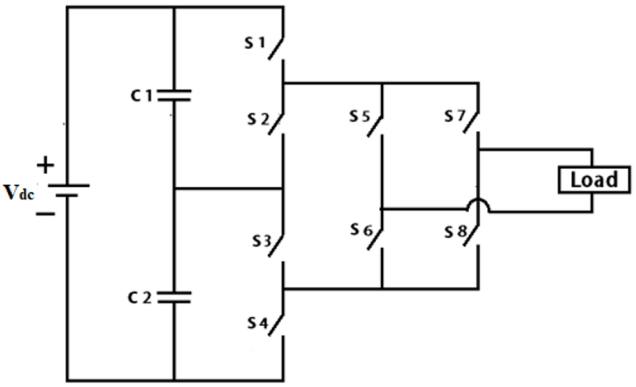


Fig.2.Main Circuit diagram

2.1. Operation of Traditional MLI

The traditional N-level Multilevel inverter is made up of 2 (N-1) switches and (N-1)(N-2) diodes. Therefore, the 7-level inverter depicted in Fig. 1 is made up of 30 diodes and 12 primary switches.

2.2. Operation of New7-level Inverter

This design is known as reverse voltage topology. Comparatively speaking, this study needed hardly any equipment's than customary studies. Additionally, it is more effective provided that the inverter has a part that runs the H-bridgeswitching electricalequipment'sat line frequencyand remaining switches are operates at high switching frequency. As a result, it is not necessary for every switch to operate at large frequency, resulting in a simpler and more dependable way to regulate the inverter.

Table.1. Turn ON switches

Voltage Level	Turned ON switches
+V dc	S1,S7,S6,S4
+2V dc/3	S1,S7,S6,S3
+V dc/3	S2,S7,S6,S4
0	S2,S7,S6,S3
-V dc/3	S2,S5,S8,S4
-2V dc/3	S1,S5,S8,S3
-V dc	S1,S5,S8,S4

Asof table.1 the level of the output of the inverter is 7-level such as $+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$,0,$-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$. As of fig.2 the dc link capacitors of C1, which charged to voltage of 2/3 of $V_{dc}$and capacitor C2 charged to voltage of 1/3 of V_{dc}. The output voltage levels are obtained by appropriate switching sequences, as shown in fig.3.(i)-fig.3.(vii).

(i) For $+V_{dc}$ level

As illustrated in Figure 3(i), switches S1 and S4 are engaged for level $+V_{dc}$ during high frequency and switches S6 as well as S7 at line frequency. The total voltage of output is equals the summation of voltage sources within the current path. As an outcome, the output is V_{dc} volt.

(ii) For $+2V_{dc}/3$ level

As illustrated in Figure 3(ii), switches S1 and S3 are engaged in level generation and switches S6 and S7 are Turned ON in polarity generation part of the inverter.

(iii) For $+V_{dc}/3$ level

As per fig 3(iii), switches S2 and S4 are engaged from level generation part switches S6 and S7 are switched ON in polarity generation part of the inverter.

(iv) For 0 level

For 0 level adjust the switches, S2, S3, S6 and S7 are turned ON as shown in fig.3.(iv). It is also possible to obtain this level with redundant path by turn ON switches S5 and S7 only.

(v) For $-V_{dc}/3$ level

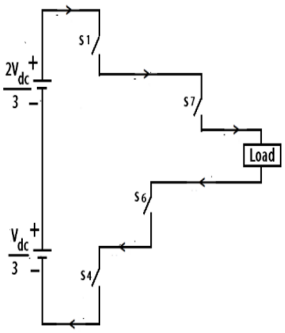
Here the switches S2 and S4 from level generation part and S5 and S8 from polarity generation part is activated to get the voltage of –Vdc/3 across the Load is shown in fig 3.(iii).

(vi) For $-2V_{dc}/3$ level

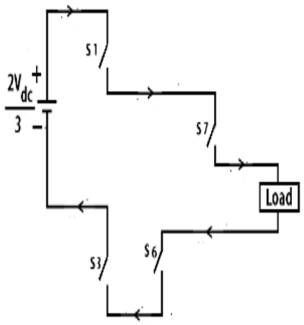
The voltage of -2Vdc/3 is appear across the Load is obtain by turn ON of S1, S3, S5 and S8 which is represented in fig.3.(vii)

(vii) For –Vdc level

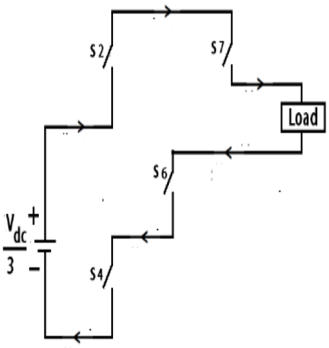
Finally the voltage of –Vdc across load is obtained by turn ON of switches S1 and S4 from level generation portion and S5 and S8 from polarity generation portion as shown in fig.3.(vii)



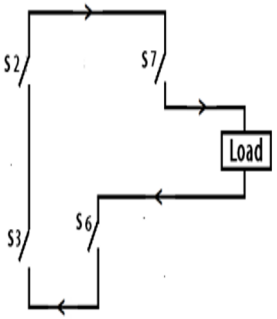
(i) $+V_{dc}$level



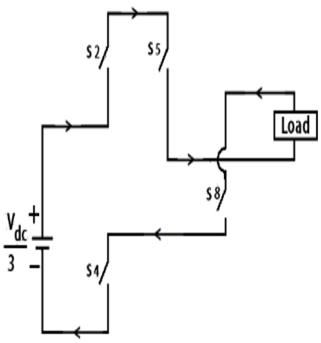
(ii) $+2V_{dc}/3$ level



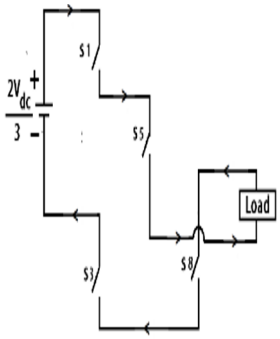
(iii) $+V_{dc}/3$ level



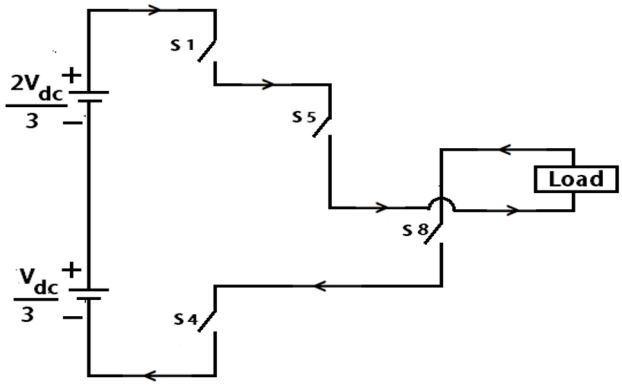
(iv) 0level



(v) –Vdc/3 Level



(vi) –2Vdc/3 Level



(vii) –Vdc level

Fig.3. Switching states of the topology

3. CONTROL TECHNIQUE

A variety of control techniques, including (i) level shift PWM, (ii) phase shift PWM, and (iii) space vector PWM, are currently used to regulate the majority of MLI. In level shift control methods, the inverter pulses are created by comparing the carrier signals with sinusoidal waves. They are once more categorized as PDSPWM, PODSPWM, APODSPWM, COSPWM, and VFSPWM based on where the carrier signals are positioned. All control techniques have a high frequency of N-1 carrier signals. One reference signal with a frequency of 50 Hz is contrasted to a carrier signal with a frequency of 2 KHz, for instance, to generate aN level output voltage and current waveform. But here only three carrier signals (fig.5) are compare with unidirectional reference wave instead of six carrier signals, as shown in fig.4. Here, a pulse width modulation technique called phase disposition is used. In this PDSPWM method all carrier signal are in phase in above reference axis. Whenever the reference signal (V_m) exceeds the carrier signal (Vc)then pulse signals are generates, which are shown in fig.6. are generated with use of XOR,OR gates for level generation portion switches.

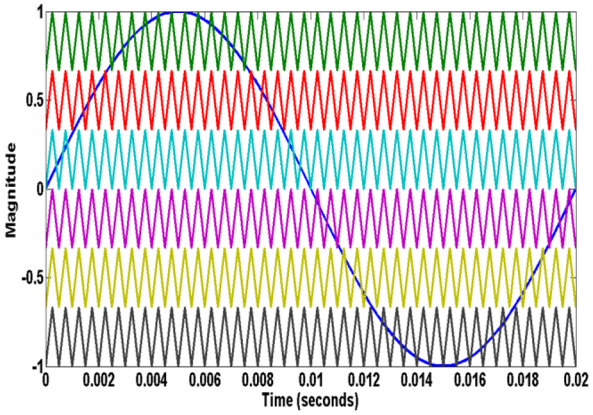


Fig.4. Phase Disposition SPWM with six carrier signals

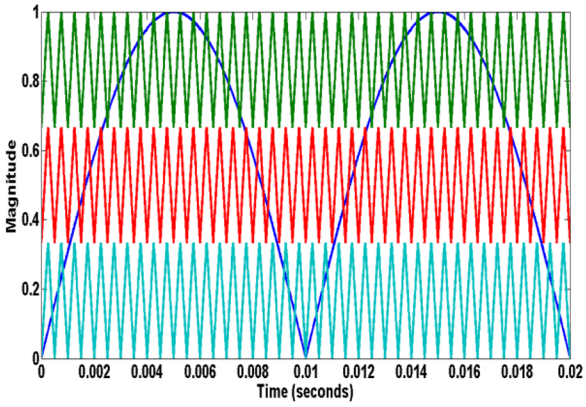


Fig.5. Phase Disposition SPWM with three carrier signals

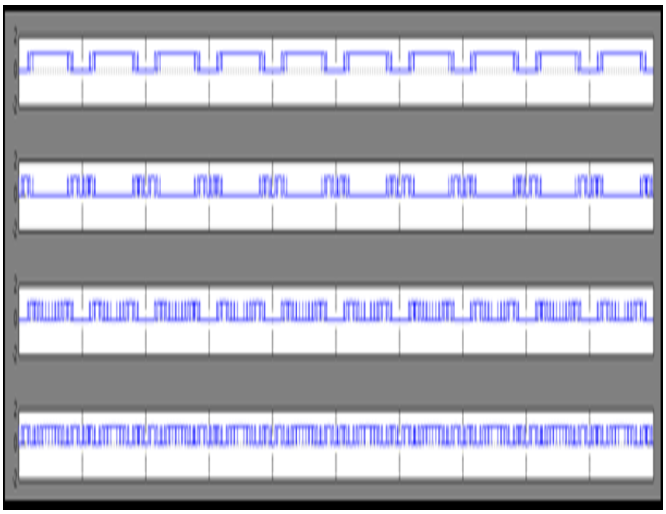


Fig.6. Pulses for the Level generation portion switches

4. RESULTS AND DISCUSSION

Table.2. Circuit parameters

S.No	Parameter	Value
1	DC Voltage source(V_{dc})	200 V
2	Load Resistance	50 Ohms
3	Load inductance	30mH
4	Modulation Index	1
5	Carrier frequency	2000Hz
6	Line frequency	50Hz
7	Output current (R- load)	4A

MATLAB/Simulink software is used to examine the inverter's performance. Depending on both switching sequences of the table 1, the inverter's output current and voltage are observed for both R-Load and R-L load.

DC input voltage of 200 V, which is split as two sources i.e 2Vdc/3 and Vdc/3, is used to generate the 200 V of AC voltageacross R-load as shown in fig.7 and the current of 4A through this load is also shown in fig.8. In order to obtain this voltage and current, here a modified SPWM technique is used. In this three carrier signals instead of six carrier signals are compared with unidirectional reference wave.

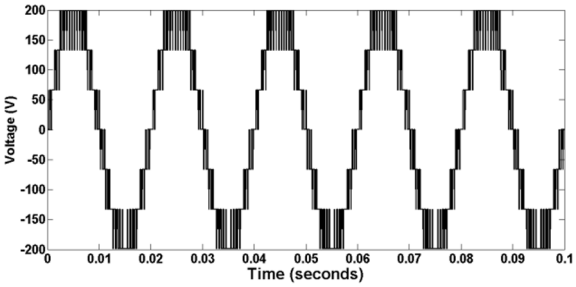


Fig.7. Voltage Response for R-Load

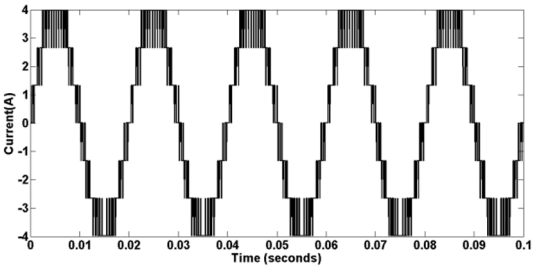


Fig.8. Current Response for R-Load

Also the response of the voltage and current through the R-L load are shown in fig 9.and fig.10 respectively. Here the magnitude of current through the R-L load is 4A .

Total Harmonic Distortion (THD) can be used to determine the quality of an inverter's output voltage and current. This voltage THD is evaluated at various modulation index values for R-load and R-L Load, as shown in the table. 3. The THD of an voltage of 200V is observed to be 13.01% for R load and 13.11% for R-L load, as shown in figures 11 and fig.12, and the THD of an output current of magnitude 4 amps, is 4.29%, as shown in figure 13.

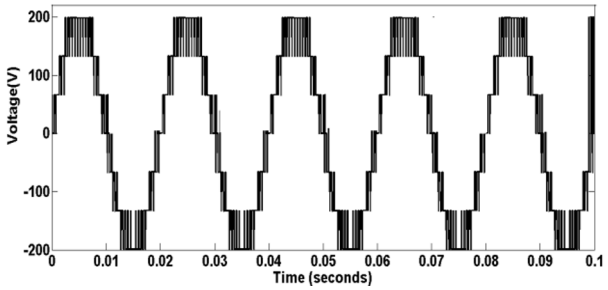


Fig.9.Voltage Response for RL-Load

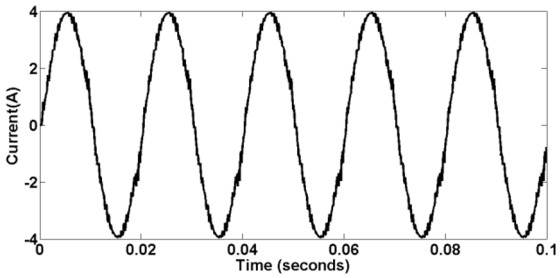


Fig.10. Current Response for RL-Load

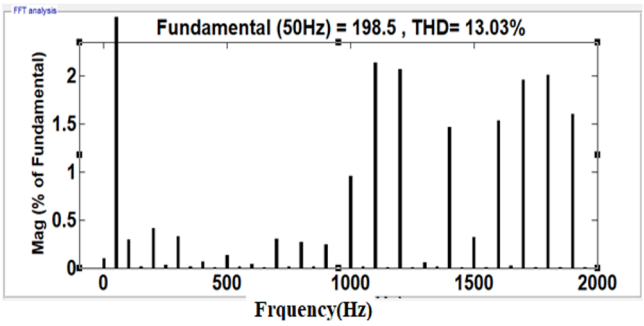


Fig.11.Spectrum of THDof output Voltage (R-load)

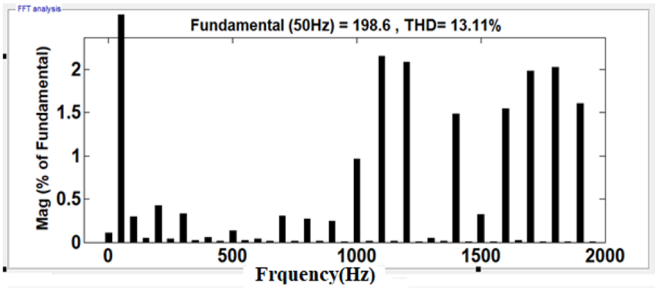


Fig.12 Spectrum of THD of output Voltage (R-L Load)

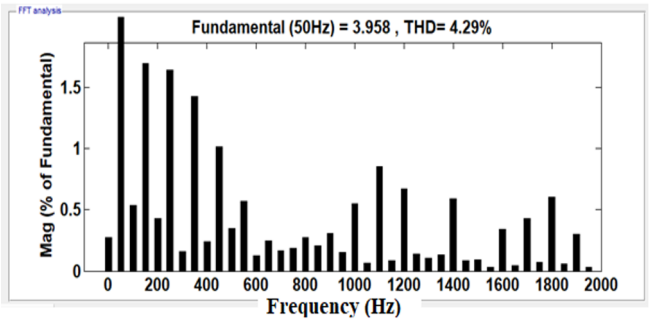


Fig.13 Spectrum of THD of output current (R-L Load)

Table.3. Variation of THD with Modulation Index values

Modulation Index Value	%THD (R-Load)	% THD (R-L Load)
0.8	18.19	18.29
0.9	17.34	17.44
1	13.04	13.11

5. CONCLUSION

Here a novel seven level inverter with less no of count devices and lower carrier signals to control the switches is demonstrated. This topology consist by two portions, one is consist by four high switching frequency devices and second portion build up by H-bridge inverteroperates at line frequency. The first part generates the levels of the output and second part generates the polarity. The controllability of the inverter is implemented by Phase disposition sinusoidal pulse width modulation technique with less carrier signals compared with unidirectional reference wave. The output voltage of seven level with less THD of 13.01% and output current of the inverter is also has less harmonics content of 4.29% is observed. MATLAB/Simulink was employed to demonstrate the inverter's design and analysis.

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