Design and Implementation of Low Power, Area Crosstalk Reduction Using Static Timing Analysis

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Abstract— One of the biggest issues with VLSI connections is crosstalk, which is caused by coupling capacitance. Crosstalk reduces operation performance during switching activities and produces undesired output. Noise level rises as switching frequency does as well. Crosstalk will be eliminated by encode the data before connecting into the bus line**.** This procedure reduces the crosstalk issue by using the improved logic architecture. The proposed approach utilizes a combination of circuit-level optimization techniques, such as gate sizing and interconnect optimization, and advanced timing analysis tools to minimize power consumption and reduce crosstalk.

Keywords—Crosstalk, Static timing analysis, Bus encoder , Bus decoder, Very Large Scale integrated (VLSI)Circuit, Crosstalk probability detector.

1. INTRODUCTION

Crosstalk is the main issue in wireless communication, integrated circuit design, structured cabling, and other communication systems. Electronics professionals are familiar with the term "crosstalk," which describes the occurrence when a signal from one band of a transmission line has an unfavourable impact on another channel. Due to reciprocal inductance between two connections, crosstalk occurs in integrated circuits. By designing of integrated circuitwe will get undesired effect that is call it as crosstalk due to the coupling capacitance the crosstalk produces [2].

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The switching properties of a net are affected by the contemporaneous switching of net that are physically near toone another because of parasitic capacitance in VLSI circuits.The analysis net that experiences coupled noise is referred toas the victim, and any nearby nets that cause pairing noise onthe defendant are referred to as the aggressors. As a result of the victim being pushed up owing to the coupling capacitance's short size, the glitch caused by the aggressor's transition is known as a coupling noise pulse. The linkage pulse can delay the victim changeover and lengthen the victim arrival time if the aggressor and victim switch in mutually opposing directions. The coupling-noise spike can shorten the victim arrival time and accelerate the victim transition if the aggressor and victim pair changes directions. Delay noiseis the term used to describe this variation in victim arrival time brought on by coupling noise. High performance VLSI circuits' circuit latency is significantly influenced by delay noise[3] .
In present fabrications of VLSI circuits are rapidly increases consequently, the capability of coupling noise prediction at the framework level is crucial if the coupling noise is not predict get the distortion signal and get undesired output and reduces the quality of the data. So by eliminating coupling noise will get desired output and produces quality of the data[5].
A circuit failure could happen if the recipient's peak noise energy exceeds the threshold voltage. On top of that, due to periodic errors inside the logic gates, the generated more power that can be transmitted on the slack line as a result of noise voltage. [4].
The operational clock frequency of VLSI chips often serves to describe their performance. Each chip may be
exposed to different operating circumstances throughout each clock cycle, including various input vectors, temperatures, and voltage profiles. Circuit designers use timing analysis as a tool to check whether such a chip can operate at the desired frequency. The objective is to ensure correct circuit operationby making sure the impulses at the circuit's output arrive at the appropriate time, meaning neither too early nor too late. Time analysis thereby promulgates the impulses to the circuit's outputs for a specific circuit layout and confirms that all timing restrictions are met. Timing verification iscommonly carried by using static timing analysis (STA).
This implementation decreases the crosstalk problem to improve VLSI circuit performance. The data can be encoded before being transmitted into the interconnects by designing a bus encoding technique

2. Literature review

Before, several techniques are used to reduce the crosstalk elimination problem. Filtering circuits that are mainly RLC-based are used to lower peaks generated by crosstalk problems and some of them work in encoding and decoding schemes to reduce the crosstalk elimination problem to encode the data before connecting to the signals to the long nets. Here are some of the previous suggestions for eliminating crosstalk which are given below.
B. Obulesu, Dr. P. Sudhakara Rao [1]Proposed the power and area constrained crosstalk elimination circuit by minimize the power and area in the VLSI connections. Due to crosstalk occurrence in conventional design the usage of power and area is more, to reduce that a proposed model is implemented
The very worst crosstalk distortion for both intra-chip and inter-chip optical connectivity systems is reviewed methodically by Luan H. K. Duong et al. In order to study theinter-chip crosstalk they employed I 2CON, they investigate both coherent and inconsistent 2nd crosstalk sounds. All network-level analytical models may be turned into machine-level prototypes using this method, starting from the bottom up, for testing. Additionally,

they calculate signal-to-noise ratio(SNR), crosstalk noise, and signal power loss[6] .
Crosstalk noise in Wavelength Division Multiplexing (WDM)-based fibre network-on-SNR chip, crosstalk noise is a major issue (ONoCs).Finding the best ONoC design to meet certain performance and scaling criteria includes assessing the worst scenario as well as the mean crosstalk noise and SNR in various ONoC architectures.M. Nikdast et al. offer a thorough systematic study and worst-case evaluation, as well as average signal strength, interference power, and SNR ratio centered on WDM cell-based ONoC, based on bold and bold bent tree using the guide and flare of the Crux optical system.[7] The studies in any WDM-based ONoC are made easier by the integration of the proposed analytical models into a Crosstalk noise and Loss Analysis Platform (CLAP). It shows that different ONoC designs result in distinct SNR presentations using quantitative simulations in CLAP. Additionally, they show that how SNR varies.
Ramesh Kumar, Vobulapuram. to examine all cross effects of VLSI connections, presented a Time-limited distribution technology (unconditional technology) (US-FDTD). A nonlinear CMOS driver that contains a leakage drive parameter and is created by the modified alpha power law model drives the interconnect lines. Capacitive loads serve as the connecting lines terminations. The projected perfect is completely stable and is not constrained by the Courant-Friedrich-Lewy (CFL) condition. For the approximation of performance factors, the projected model yields an average percentage error <1% [8].
Srinivas Katkoori and Hariharan Sankaran In tire-based macro cell designs, it offers a high-level integration structure to reduce the worst incidence. Before making any physical adjustments, the crosshair can also be removed. The transition model, which includes the Miller Coupling Factor (MCF) 4, is the worst-case cross-correlation model in the double-attack model (HLS). They develop effects depend on steel modelling (SA), which region development had forecast. They also provide a series of carrier lines, a conscious cross traffic that functions in the opposite direction as reverse encryption traffic, and a set of movements (planning, assigning, and bindings) for each HLS task. Nine DSP standards were used in these investigations. In the worst-case scenario, the suggested strategy decreased the number of crossroads from 27percent to 82percent and the number of buses by 75percent [9].
Xu Jingyu, et al. [10] proposed a method for minimizing the complexity of finding a solution without cross-track in detailed routing by developing approaches for dealing with crosstalk from a global perspective. This strategy functions as follows: To lessen congestion and improve delays, the time relaxation strategy is used early. A Crosstalk control mechanism is created in the final phase to obtain a workable crust talk solution. Our method reduces crosstalk by eliminating the high visibility area through topological optimization, using a conservative Crostalc model.

3. PROPOSED MODEL

In this paper, a bus encoding strategy is suggested as a solution to the crosstalk problem. Here, the bus data will be encoded depending on the crosstalk model to remove the mutual inductance issue present in the interconnects. The method below gives an overview of the bus encoding strategy that has been suggested and the accompanying crosstalk model that has been employed.

Crosstalk model

Considering the crosstalk model is one of the main justifications for applying bus encoding scheme design. In this model, bus encoding is used to solve the crosstalk issue. In this model, a 4-bit bus is considered for eliminating crosstalk problem. Fig. 1 depicts the RC

model for the bus encoding approach. Consumption of power in bus encoded data is shown in below:

$$Pcoded = f.(T_S C_L + T_C C_C)V^2 \quad (1)$$

$$= f.(T_S + \lambda T_C)V^2 \quad (2)$$

Where V_{DD} is defined as the supply voltage, f is the clock frequency, C_L is the load capacitance, C_c is the coupling capacitance The distinct capacitance ratio λ is as follows.

$$\lambda = C_C / C_L \quad (3)$$

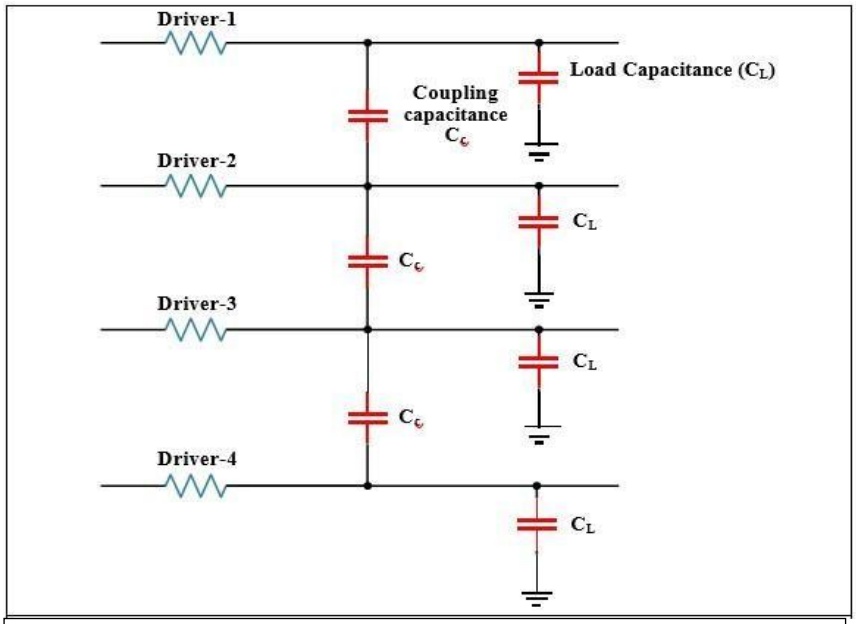

Fig.1. Crosstalk model

The cost is influenced by the technology. For instance, the value is influenced by joint width, distance, percentage, and dielectric thickness. The average values of active switching for carrying capacity are shown in equation (1) by TS, while the average readings of communication activities are shown by TC. The TS value, however, lies between 0 and 1. The TS value that is not encoded is 1. The TC value likewise falls between 0 and 1. Similarly, uncoded TC has a value of 1. Three bits from adjacent lines are compared in the activity to discover their differences.

$$C_{eff} = Cc \left| \frac{\Delta V_2 - \Delta V_1}{E} \right| + Cc \left| \frac{\Delta V_2 - \Delta V_3}{E} \right| \quad (4)$$

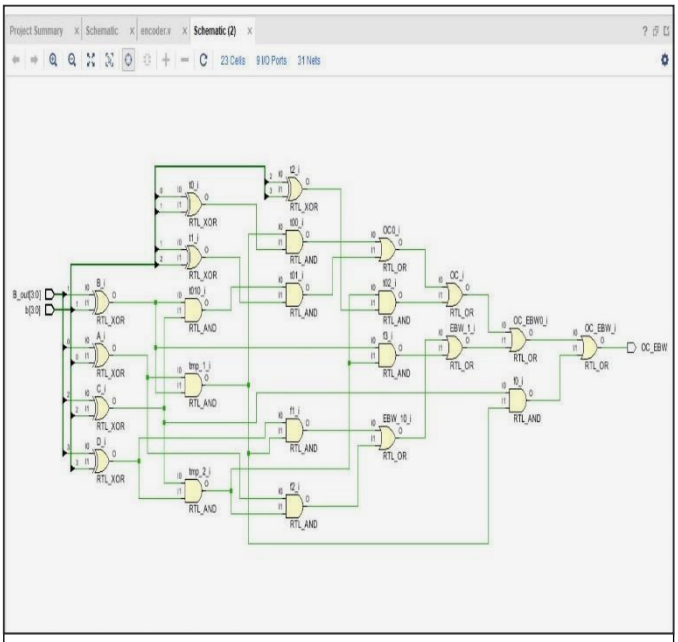

Fig.2. Schematic diagram for Crosstalk Probability Detection Model

B) Proposed Bus encoding technique

In this proposed method to avoid crosstalk problem, a bus encoding scheme is implemented. The block diagram for the proposed technique is shown in Fig.3. A very less number of components are used in this proposed technique as shown in Fig.3. The suggested method makes use of a selector module, a buffer, and a crosstalk probability detection circuit. Area, Time and power constraints are more taken into account in this design.

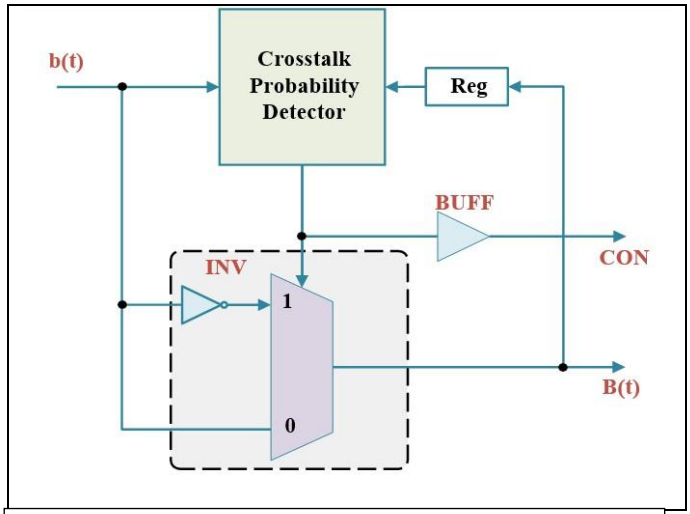

Fig.3. Proposed Bus encoder model

The crosstalk probability detector model as shown in Fig.2. this circuit model is made of AND, OR, NOT and XOR logic gates and it act as comparator. The previously encoded output is connected to the probability detector it detects the probability of the crosstalk and its output is named as selection line to the selector.
The output that has already been encoded is saved in a different register bank. The 4-bit shift register is regarded as a memory component for the purpose of storing the encoder's output data. The current encoded outcome can be constructed using the existing bus data input and already decoded output. To conduct the decoding operation, a different CON control signal will be delivered to the receiver. The encoder side will produce the output based on the choice. Based on the generated decision, a selection module is built to reverse the input. The option that comes from the decision block will be used to generate the control signal CON. The decoder will use this to carry out the decoding procedure depending on the encoded data and the decision.
The following equation shows the mathematical expression for the encoding process.

$$\begin{aligned} &\text{if (OC\_EBW == 1)} \\ &\quad B(t) = \text{NOT } b(t) \\ &\quad CON = 1 \\ &\text{else} \\ &\quad B(t) = b(t) \\ &\quad CON = 0 \end{aligned} \tag{5}$$

According to the equation (6) the decoding operation will be performed out. When CON is true inversion operation will be performed otherwise the output is consider as the same data as input. The block diagram for the bus decoding process as shown in Fig.4.

$$\begin{aligned} &\text{if (CON == 1)} \\ &\quad b(t) = \text{NOT } B(t) \\ &\text{else} \\ &\quad b(t) = B(t) \end{aligned} \tag{6}$$

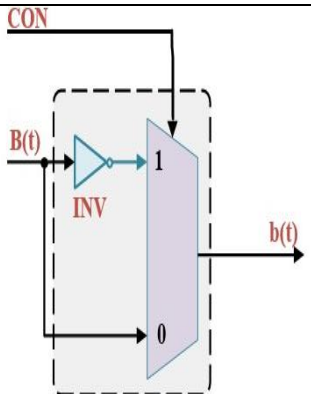

Fig.4. Bus decoder

4. RESULT AND DISCUSSION

The project is done in the Xilinx vivado software tool with Verilog programming language. The proposed bus encoder technique have three blocks, they are cross talk probability detector, selector and register. After compiling the code a simulation waveform of bus encoder is generated, according to Verilog code the schematic diagram and synthesized diagram is also generated. The design performance is measured using its power, area and time, after implementation the power, area and timing report will be obtained. The timing report is show in Fig.5. worst negative slack(WNS) is 1.713 ns, worst hold slack(WHS) is 0.166 ns and worst pulse width slack(WPWS) is 9.500 ns and the total negative slack(TNS), total hold slack(THS), total pulse width slack is equals to 0 ns. Finally the user specified timing constraints are met and there is no delay

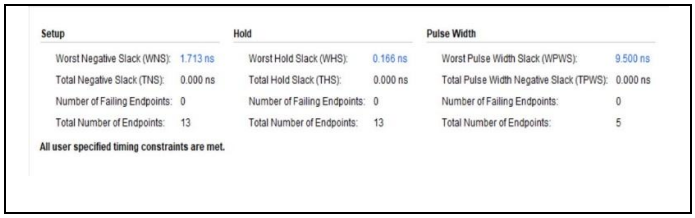

Fig.5. Timing report

The area report of the proposed method is shown in Fig.6.total 27 cells are used in these proposed method they are 11 LUT, 4FF and 12IO compare to conventional design the area of the proposed architecture is reduced and the percentage of the area is also shown in Fig.6.

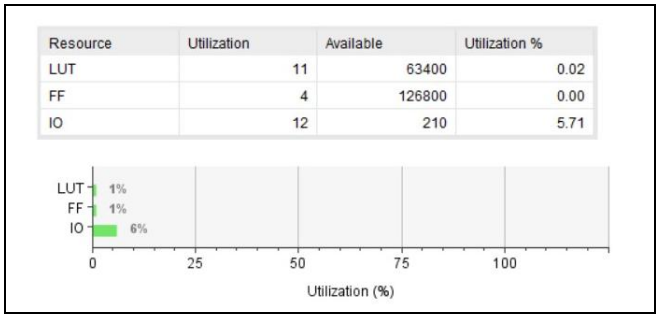

Fig.6. Area Report

The power report of the proposed design is shown in Fig.7. By allocating output load(capacitor) is 0.001pF, junction temperature is 25.383^{o}c, ambient temperature is 25^{o}c and effective thermal resistance is 4.563^{o}c/w then the total on-chip power is 0.149w as compared to conventional design the power of the proposed design reduces. As the changing of the output load the power changes. The device static power is 0.144w(97%) and dynamic power is 0.005w(3%) it is shown in Fig.7.

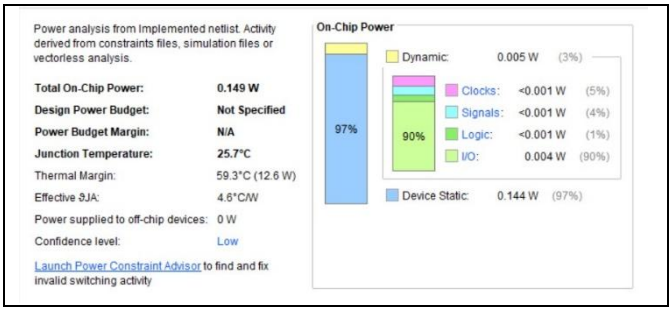

Fig.7. Power report

The proposed method simulation results is shown in below figures.

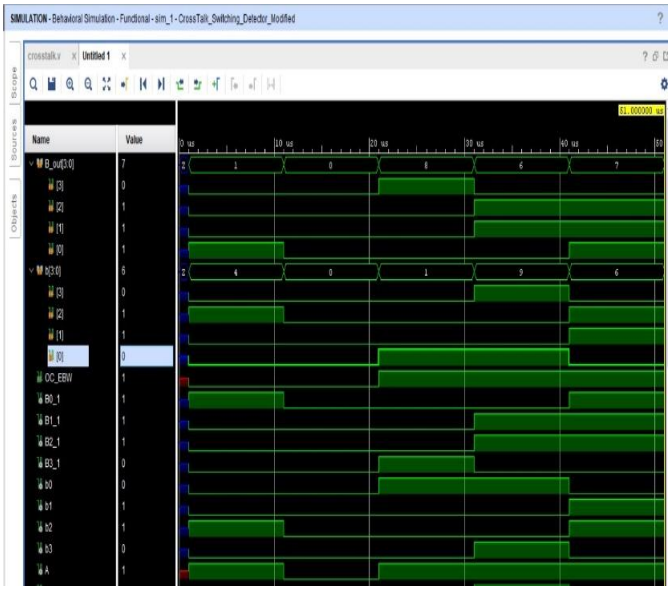

Fig.8. Simulation waveform for crosstalk probability detector

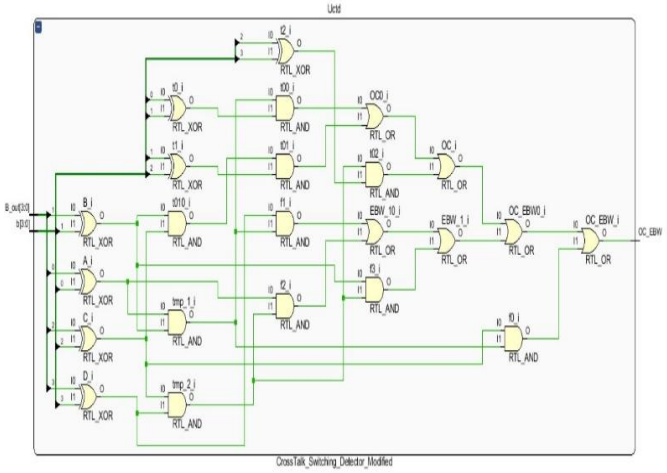

Fig.9. schematic diagram for crosstalk probability detector

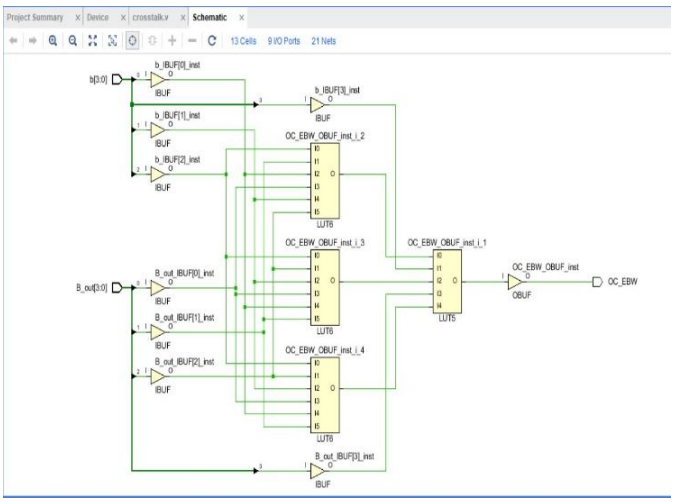

Fig.10. Synthesized diagram for crosstalk probability detector

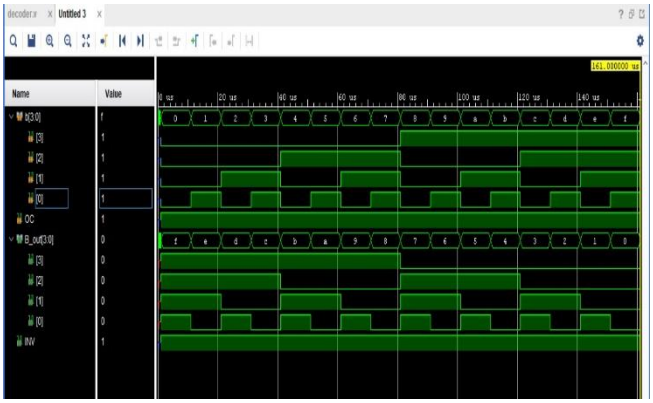

Fig.11. Simulation waveform for 2:1 selector

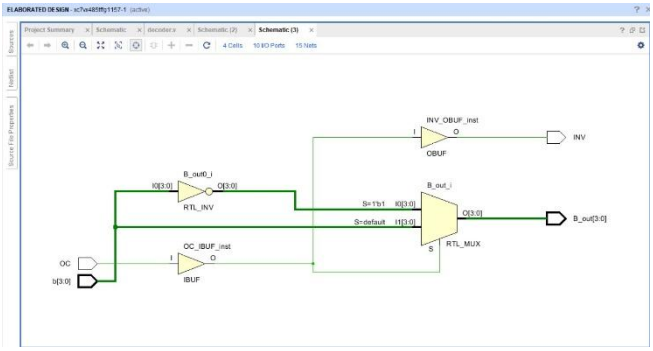

Fig.12. Schematic block diagram for 2:1 selector

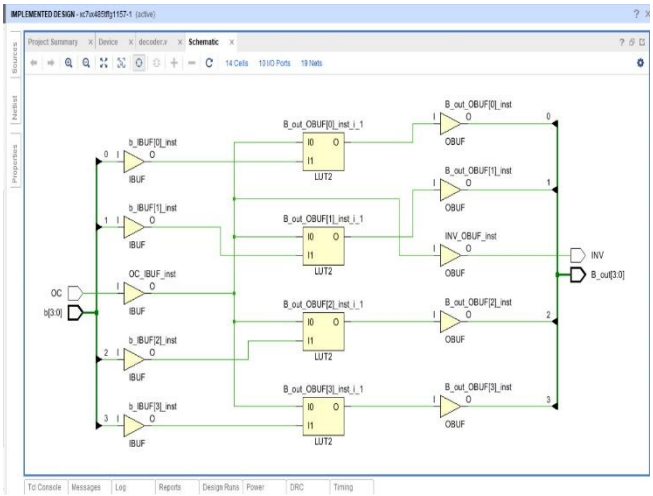

Fig.13. Synthesized diagram for 2:1 selector

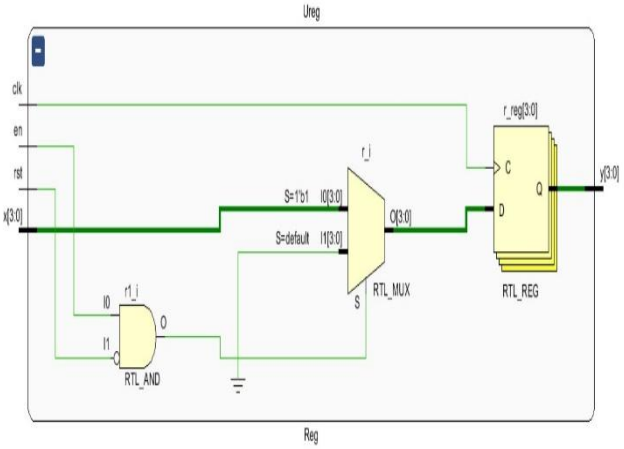

Fig.14. Schematic diagram for 4-bit shift register

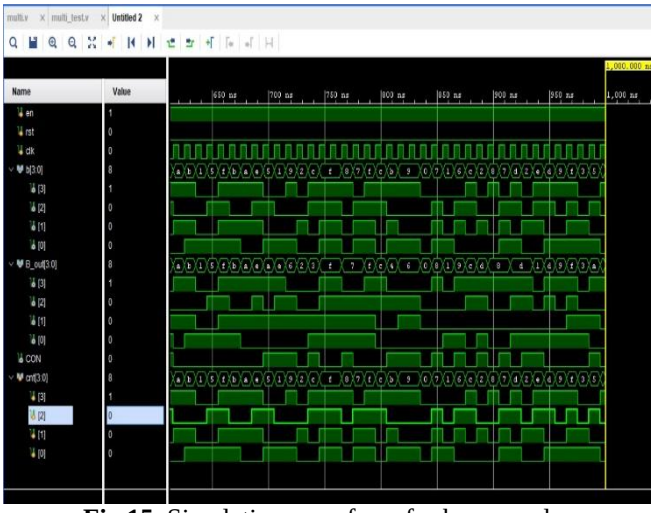

Fig.15. Simulation waveform for bus encoder

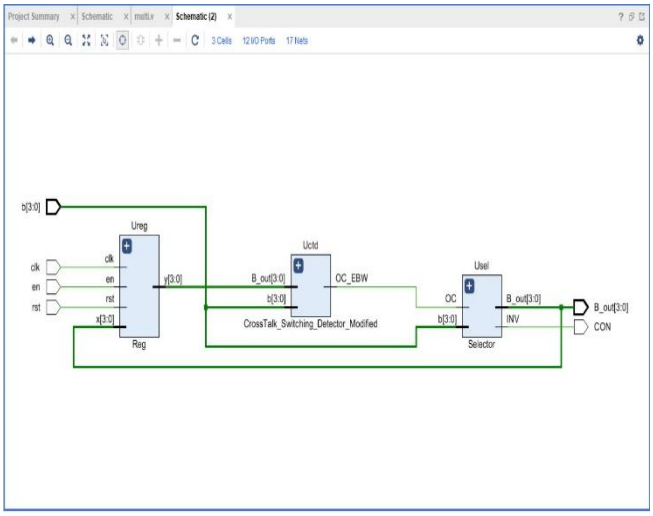

Fig.16. Schematic diagram for bus encoder

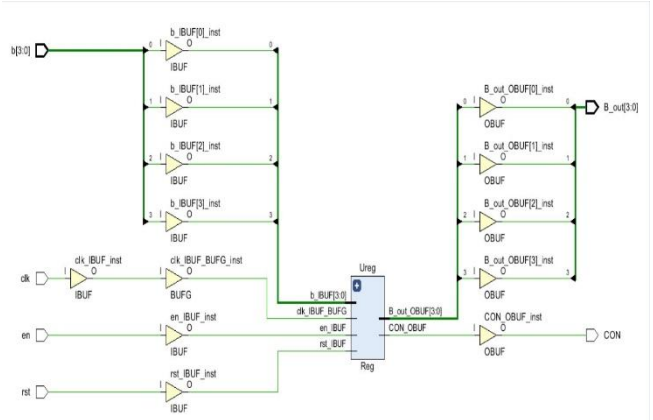

Fig.17. Synthesized diagram for bus encoder

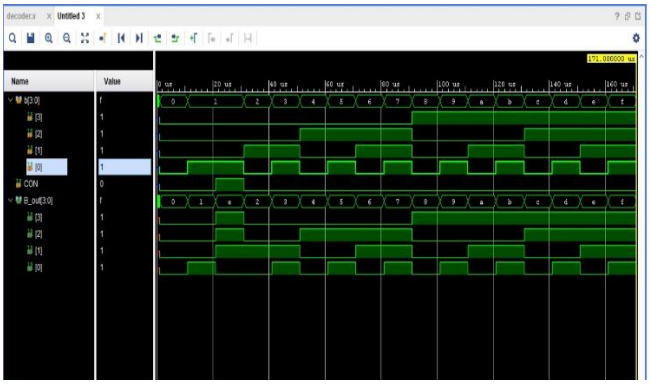

Fig.18. Simulation for bus decoder

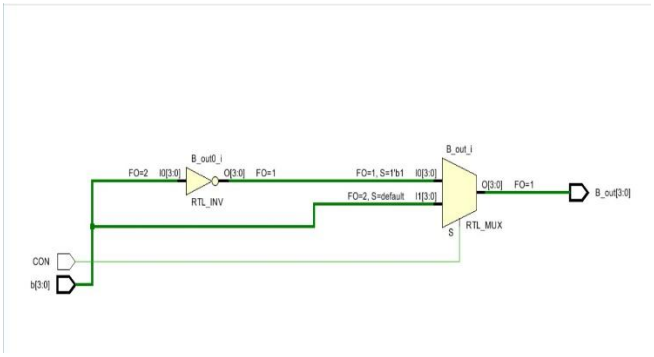

Fig.19. schematic for bus decoder

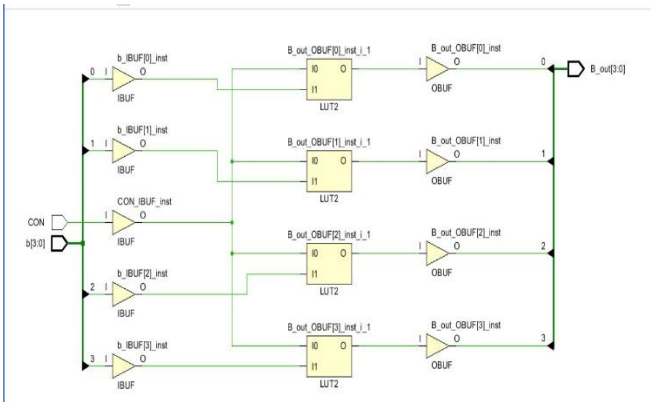

Fig.20. Synthesized diagram for bus decoder

5. CONCLUSION

Crosstalk is eliminated in VLSI interconnects by implementing bus encoding technique. By eliminating crosstalk, a desired output is produced in VLSI circuits. In this design, very few hardware components are used to build it. As a result, the design uses less area, power consumption and time. By considering the work results, the time constraints are met, area utilization is 24 cells and power is 0.149w are produced. The proposed method was shown to be effective in reducing crosstalk, power consumption and area compared to a conventional design. The design is developed in the Xilinx Vivado 2018 software.

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