Simulation of Hybrid Boost Converter with Reduced Switch Stress for PV Systems

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Abstract. Currently, there is a growing prominence on using switched capacitor and switched inductor techniques in high-power boost converters to achieve higher voltages. This is accomplished by employing reactive elements, where the inductor discharges while the capacitor charges. The switched capacitor and switched inductor can extremely attain dc voltage obtain with require few quantities like inductors, capacitors, diodes, and a switch. Modifications were made to the switched inductor converter, resulting in a reduction in the voltage stress on the active switch. The converter now operates based only on the duty ratio. This study suggests adjustments to the switched capacitor and switched inductor converter to decrease the stress on the switch by altering the duty ratio closer to unity. The paper covers the converter's operation, waveforms, design equations, and simulation results to illustrate this modified converter setup.

1 Introduction

In the modern previous years, interest closer to utilising of renewed power sources to develop electrical energy has significantly improved throughout the global. On the other hand, the renewable power sources produce a comparatively lower output, which is insufficient for fulfilling all the requirements. Hence, there is a need for a specialized, environmentally friendly, and high-power boost converter to be incorporated into the device for efficient operation. The availability photo voltaic irradiation the solar system used in low-power and medium functions [1-4]. The-isolated converter a transformer is used to physically an electrically separate the circuit into two sections. The current won't flow between input and output due to this separation and galvanic isolation input and output use as the same ground reference in non-isolated circuit. Non isolated converter does not have a transformer and does no longer require any physical separation between input and output, so this generally makes them smaller and lighter. It also additionally improves efficiency as there is no transformer losses to take into consideration.

In literature review, the different converter topologies are introduced based on a boosting-methods [5-8]. When a converter has isolation transformer, then the converter is capable of withstanding high voltage ranging from a few hundred to several thousand volts, which is generated at the output of converters like the flyback, push-pull, and H-bridge. Inductor coupled and capacitor coupled converters are presented then increases voltage and reducing ripple content and reducing the voltage stress across the semiconductor devices [9-11].

2 Proposed Converter

This proposed converter is derived from basic boost converter and its topology is modified by cascading various voltage boost networks. Fig. 1 depicts the proposed converter topology. The main drawback of the increasing the number of voltage multiplier (VM) cells results in more losses in the semiconductor devices. The voltage lift technique stands as a mostly used method in electronic circuit design. This method also can be used for enhancing the voltage gain of DC-DC converters. A voltage lift circuit consists of inductors and capacitors as energy storage components in the converter circuit. Hence, for achieving increased voltage gain while minimizing the count of voltage multiplier cells, the basic simple switched inductor (SI) cell is modified. The detailed operating principle will be explained in the following sections.

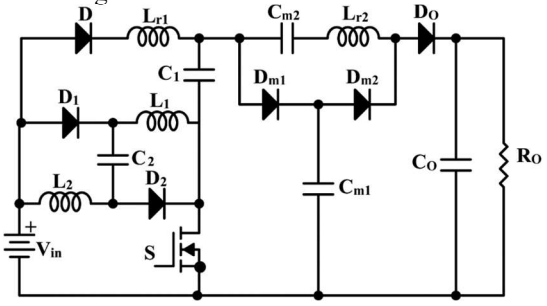

Fig. 1. Topology of proposed converter

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2.1 Operating Principle

The voltage lifted switched inductor cell is formed by inductors L1, L2, the diodes D1, D2, and capacitor, C2. Both inductors, L1 and L2, has an identical value of inductance designated as "L." Similarly, the capacitance value of the capacitors C1 and C2 are presumed to have same value, and it is denoted as "C." Capacitor C1 functions as the switched capacitor cell in the proposed converter topology.

Resonant inductors play a decisive role in switched capacitor network and voltage multiplier cells by predominantly aiming to alleviate the current peak generated by the capacitors. During the charging period, the SI and switched capacitor (SC) cells are connected in parallel with the input voltage source, while during discharging, they are connected in series. The resonant inductor forms a tank circuit with the capacitor C1. The proposed converter topology has four distinct operating modes, which are illustrated in Fig. 2 – Fig. 5 and explained in the following sections. Figure 6 depicts the theoretical waveforms corresponding to the proposed converter topology.

During mode 1, the power switch, S, is turned off and it is depicted in Fig. 2. The capacitor C1 and the switched inductors L1 and L2 are connected in series with the input voltage source, Vin. The energy, which was stored in switched capacitor, C1 is discharged to multiplier cell capacitor, Cm1 and subsequently to the output capacitor, Co. Simultaneously, resonant inductor Lr2 current is increased, while the multiplier diode (Dm1) current is reduced, whereas the change in current follows a linear progression.

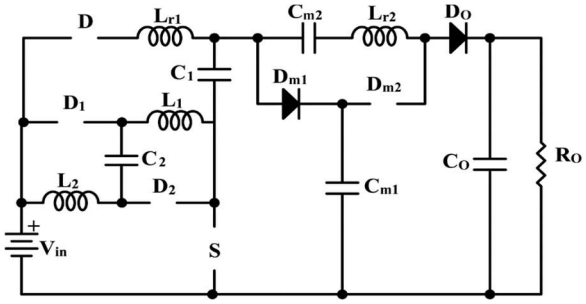

Fig. 2. States of semiconductor devices in Mode 1

During mode 2, at instant t1, the current through Dm1 reaches zero, while the currents in Lr2 and SI cell become equal. The stored switched inductor energy is transferred to the load, as depicted in Fig. 3. In both modes 1 and 2, the capacitors and inductors of the voltage lifted switched inductor cell, and the input voltage source are interconnected in series, discharging their stored energy to the load resistance. Consequently, the current flowing through C1, C2, and L1 remains identical.

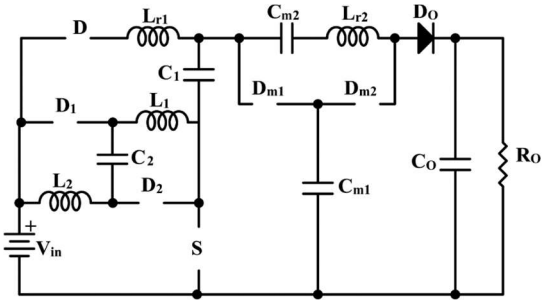

Fig. 3. States of semiconductor devices in Mode 2

During mode 3 operation, the switch is turned on a time t2 and the equivalent circuit the converter with forward biased and reverse biased diodes are shown in Fig. 4. A LC tank circuit is formed, and the sinusoidal current occurs causing the inductor current to increase.

When the magnitude of the sinusoidal current oscillations reaches zero, the diode becomes reverse biased. Subsequently, the stored energy in capacitor is transferred to voltage multiplier cell.

During mode 4, the switch S remains conducting, leading to a further increase in the switched inductor cell current. As the capacitor is completely charged, no current flows through it.

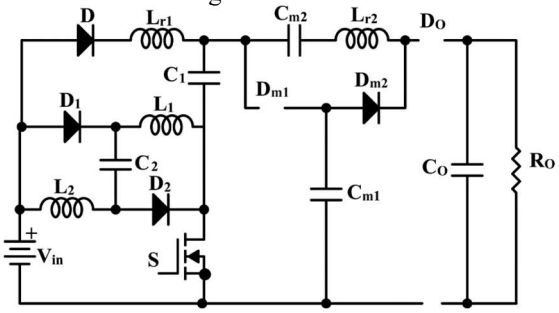

Fig. 4. States of semiconductor devices in Mode 3

Likewise, at t3, the resonant inductor Lr2 exhibits zero current, causing the reverse biasing of the volage multiplier cell diode Dm2, as depicted in Fig. 5. This mode will continue until the switch is turned off.

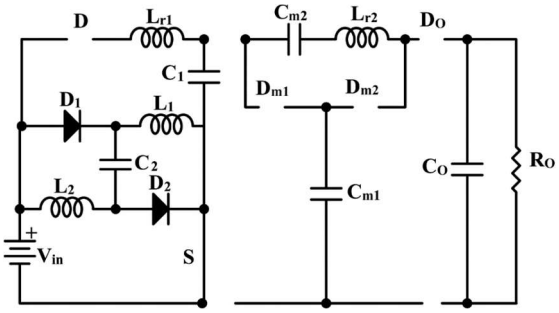

Fig. 5. States of semiconductor devices in Mode 4

The voltage available across the switched inductor cell i.e., L1 or L2 can be determined by applying the theory volt-second balance principle and it is used to determine the converter voltage gain of the proposed topology.

$$D V_{in} = (1-D)\frac{V_{Cm1} - 3V_{in}}{2} \quad (1)$$

$$V_{Cm1} = \frac{(3-D)V_{in}}{1-D} \tag{2}$$

$$V_{Cm2} = \frac{2}{1-D}V_{in} \tag{3}$$

$$M = \frac{V_O}{V_{in}} = \frac{5-D}{1-D} \tag{4}$$

The converter's voltage gain versus the duty cycle characteristics curve of the proposed converter circuit is shown in Fig. 7.

The voltage stress available on the active switch, S and the power diodes of the proposed topology are determined by the following equations.

$$V_S = V_{Cm1} - V_{C1} = \frac{2}{1-D}V_{in} \tag{5}$$

$$V_{DO} = V_{Dm1} = V_{Dm2} = \frac{2}{1-D}V_{in} \tag{6}$$

$$V_{D1} = V_{D2} = \frac{V_{in}}{1-D} \tag{7}$$

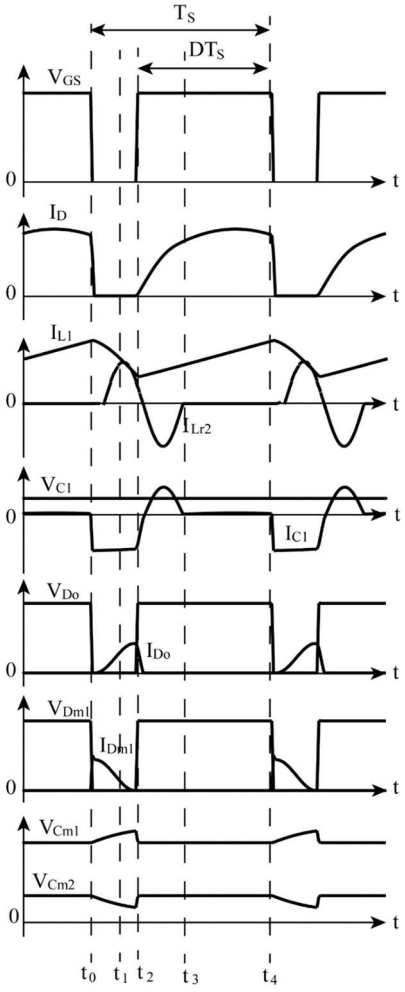

Fig. 6. Typical steady state waveforms

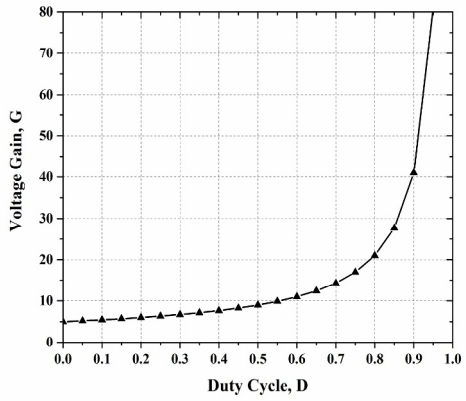

Fig. 7. Converter's voltage gain vs. duty cycle

The expression for capacitances presented in the proposed converter is given by

$$C_1 = C_2 = \frac{I_{O-\max} T_S}{\Delta V_C} \tag{8}$$

$$C_{m1} \geq \frac{P_{O\max} \cdot T_S}{V_{Cm1}^2} \tag{9}$$

The inductance value of resonant inductor Lr1 SI inductors L1 and L2 can be calculated by using the below equations.

$$L_{r1} = \frac{1}{4\pi^2 f_O^2 C} \tag{10}$$

$$L_{r2} = \frac{V_O - V_{Cm2} - V_{C1}}{\Delta I_{Lr2}} \tag{11}$$

$$L_1 = L_2 = \frac{V_{in}}{\Delta I_L} D_{\max} T_S \tag{12}$$

The proposed converter is designed as per the design equations given above for the specifications presented in Table 1. The gain and duty cycle for given nominal input voltage are calculated as Gain, M = 15 and nominal Duty cycle, D = 0.714. The maximum value and minimum value of duty cycle required for the given input voltage variation is Dmax = 0.814 and Dmin = 0.6097.

3 Results and Discussions

The main system parameters of the proposed converter were tabulated in Table 1 and they are used in the simulation. The PSIM simulation layout model of the suggested high step-up converter topology is shown in Fig. 8. Throughout the simulation, a constant input voltage and a steady load were used. Consequently, the duty cycle is maintained constant. Nevertheless, a simulation was run and the load was changed gradually in steps to assess the proposed converter's dynamic behaviour.

Table 1. Design Specifications and parameters calculated for the proposed converter topology

System parameters	Specifications
Switching frequency, fs	100kHz
Load voltage, Vo	360V
Output power, Po	500W
Input Voltage, Vin	24V
Inductors	$L_1 = L_2 = 100\mu H$
Resonant inductors	$L_{r1} = L_{r2} = 0.22\mu H$
Capacitors	$C_1 = C_2 = 33\mu F/100V$ $C_{m1} = C_{m2} = 1\mu F/500V$ $C_O = 100\mu F/500V$

Fig. 9 shows that the switching frequency is 100 kHz, and the average input power is about 500W. Fig. 10 shows the waveforms of the current flowing through the capacitors, C1 and C2, and the voltages across the capacitors C1, C2, Cm1 and Cm2. The capacitor voltage V_C1 and V_C2 are almost equal to the input voltage, Vin and the multiplier capacitor voltages are equal to the theoretical values.

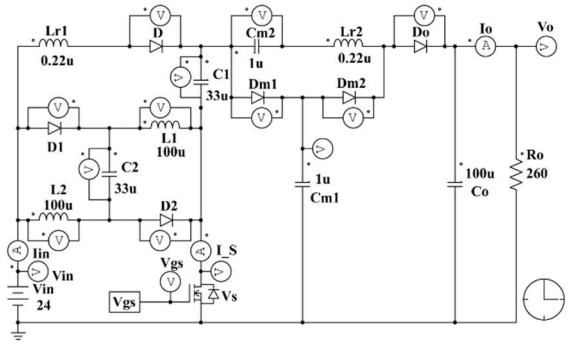

Fig. 8. Simulation model of proposed converter topology

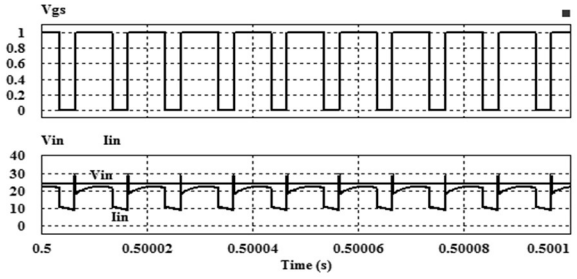

Fig. 9. Switching signal, input voltage and current waveforms during simulation

Fig. 11 illustrates the waveforms of the instantaneous voltage and current in the power switch, S and the diode, D. It can be seen from the simulation that the switch, S operates with soft switching. Since the diode and resonant inductor Lr1 are in series, both carry the same current.

Fig. 12 shows the voltages and currents presented in the multiplier cell diodes and switched inductor diodes. Due to the presence of resonant inductor and capacitor across the diodes, the diode current is sinusoidal in nature.

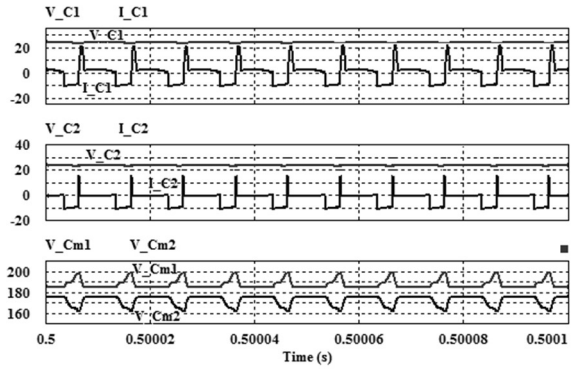

Fig. 10. Currents in C1 and C2, and voltages across C1, C2, Cm1 and Cm2 during simulation

Fig. 13 shows the load voltage and load current at rated power. The dynamic performance of the suggested converter architecture is shown in Fig. 14. The load is varied in steps and maintains the same for a specific interval. Initially, the load of the converter is at 80% of the rated power and the load is increased to 100% rated power at 0.6 sec and once again the load is increased to 120% of the rated power at 0.85 sec.

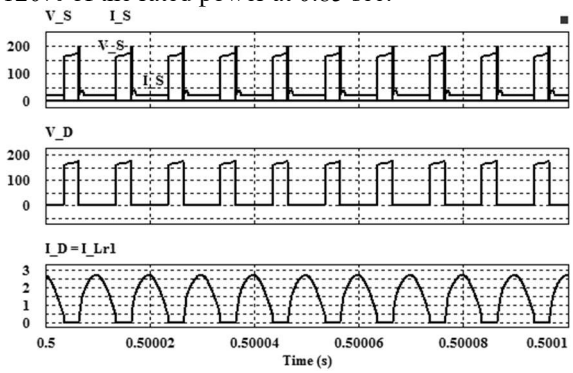

Fig. 11. Voltages and currents in switch, S and diode, D

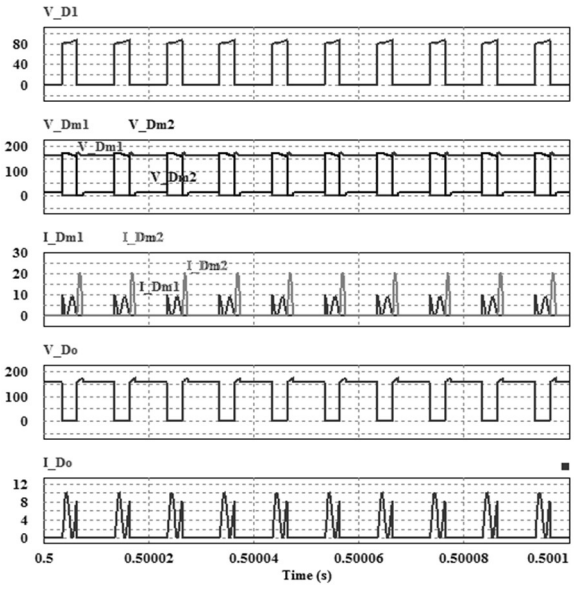

Fig. 12. Voltage and current in diodes during simulation

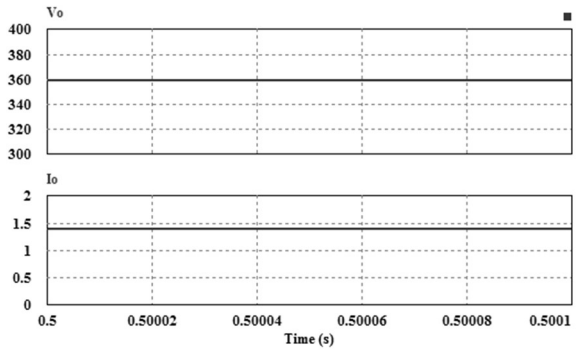

Fig. 13. Load voltage and current waveforms

In all load conditions, it is obvious that the voltage is maintained at rated value and its regulation is at acceptable level. The conversion efficiency is more than 90 % over the wide variation of load and maximum efficiency is 93 %.

The performance parameters obtained from simulation results is given in Table 2. Since the devices used in the PSIM are ideal, the other losses are zero. Hence there will be small variation between the simulated values and experimental values. The losses in the devices can be reduced by selecting low on-state resistance MOSFET and fast switching diodes. But the cost of the devices is high. Hence, the devices must be selected properly without compromising the performance of the converter.

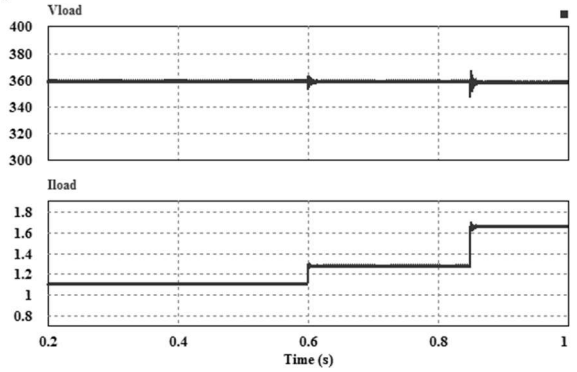

Fig. 14. Dynamic behaviour of the proposed converter topology

Table 2. Performance Parameters of Proposed Converter

Parameters	Simulated values
Power loss in MOSFET	28.34 W
Total power loss in diodes	14.9 W
Converter efficiency	92.04 %
Voltage across the switch, S	174 V
Capacitor voltage, C2	24 V
Capacitor voltage, Cm1	191.8 V
Capacitor voltage, Cm2	168.2 V

4 Conclusions

In this paper, the topology, operating modes, theoretical waveforms, operational analysis, and design considerations such as voltage gain, voltage stress across the switch and the diodes are given. This proposed hybrid converter enables efficient high step-up operation. The proposed structure allows even higher output voltage levels only by cascading a greater number of voltage multiplier cells. The suggested converter functions in ZCS mode, according to the steady state study of its functioning. This represents an advantageous operational state, contributing to the converter's efficient performance and showcasing its potential for high-voltage operations while minimizing energy loss during switching transitions.

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