Design and real-time implementation of novel reduced-switch 7-level multilevel inverter

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Abstract. This paper presents the design, simulation, and experimental validation of a high-efficiency, reduced-switch seven-level multilevel inverter (MLI) utilizing an Arduino-based control strategy. While traditional multilevel topologies—such as the Cascaded H-Bridge (CHB)—offer superior power quality, they are often constrained by high component counts, increased switching losses, and complex gate-drive requirements. The proposed topology addresses these limitations by employing a strategic configuration of only eight power switches and a single DC source integrated with a capacitive voltage divider network. This optimized structure significantly reduces the semiconductor footprint and simplifies the auxiliary circuitry required for level generation.The system performance was initially evaluated through MATLAB/Simulink to analyze the total harmonic distortion (THD) and switching transitions. Subsequently, a hardware prototype was implemented using IRF540N MOSFETs, TLP250 opto-isolated gate drivers, and an Arduino UNO for pulse-width modulation (PWM) execution. Experimental results demonstrate the successful generation of a seven-level stepped waveform with a measured THD of 8–10%, aligning closely with simulation data. The findings conclude that the proposed inverter offers a robust, cost-effective, and compact solution for low-frequency AC applications, renewable energy integration, and small-scale industrial drives.

1 Introduction

In recent decades, Multilevel Inverters (MLIs) have become a promising alternative to conventional two-level inverters in medium- and high-power applications. Not like traditional inverters produce a square output, MLIs generate voltage profiles by integrating several intermediate DC levels. This significantly improves the quality output waveform, reduces THD, and lowers the stress of voltage across semiconductor devices. As a result, the MLIs have been widely applied in many, FACTS devices, motor drives and power conditioning units, renewable energy systems.Many topologies of MLIs have been proposed, including the Diode- Clamped, Flying Capacitor, and Cascaded H-Bridge configurations. Among these inverter, the cascaded H-Bridge inverter is considered the most because to its modularity and scalability. However, the main cons of CHB-based MLIs is that a huge number of power semiconductor devices and requires multiple isolated DC sources. Circuit complexity increases and cost of hardware, driver requirement, and overall losses by switching. Also the control of multiple switches becomes challenging along with the higher output levels [3, 6, 11, 12].

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To address these problems, researchers investigated reduced- switch multilevel inverter topologies that aim to use fewer semiconductor devices and to generate same number of output voltage levels with These topologies simplify the circuit structure, minimize gate driver requirements, and improve overall efficiency. By reducing the component count, such designs also offer better reliability and cost-effectiveness, and making them compatible for practical implementation in low- and medium-power applications.1, 2, 9, 10]. Here in this paper, a novel 7-Level Reduced-Switch Multilevel Inverter (7L-RSMLI) is proposed and hardware is implemented. The inverter built here utilizes a single DC source in combination with a voltage divider capacitor arrangement to generate voltage levels[intermediate]. The H-Bridge stage is then employed to alternate the polarity and produce 7 stepped output. In proposed design made use of eight switches and eight gate drivers, in contrast to conventional cascaded H-Bridge that demands twelve switches and multiple isolated DC sources. Hence reduced hardware cost, simplified control, and lower power losses.nTo validate the effectiveness of the design, the system has been modeled in MATLAB/Simulink and tested. Furthermore, a hardware Setup was built using IRF540N MOSFETs, TLP250 [optically isolated] gate drivers, and an Arduino UNO microcontroller for PWM signal generation. Simulation and experimental results have confirmed that the inverter successfully produces a seven-level stepped sinusoidal output with significantly reduced THD compared to conventional configurations.

2 Contribution and highlights

This paper extends the earlier simulation-only study of a reduced- switch 7-Level Multilevel Inverter (7L-MLI) by presenting its real- time hardware implementation and validation. The key contributions are.

1. Hardware Prototype Development – A practical 7L-MLI was designed and implemented, demonstrating reduced switch count and simplified driver circuitry.
2. Microcontroller-Based Control – An Arduino UNO (ATmega328) is programmed to generate optimized PWM switching sequences (1666 μs intervals for 50 Hz), enabling cost-effective and flexible control.
3. Simulation vs. Experimental Validation – Hardware results are compared systematically with MATLAB/Simulink simulations, confirming the reliability of the proposed topology.
4. THD and Performance Analysis – Experimental results has shown significant reduction in Total Harmonic Distortion (THD), validating the output quality and efficiency improvements of the reduced-switch design.
5. Application Potential – The work establishes the suitability of the proposed inverter renewable energy systems, for electric vehicle drives, and grid-ready applications, bridging the gap between theory and practice.

3 Methodology

The proposed inverter topology integrates a voltage divider stage and an H-bridge stage to produce seven distinct output levels: 0, ±Vi/3,±2Vi/3, and ±Vi. A capacitor divider splits the input DC source into fractional voltage levels, which are then recombined through the H-bridge stage. The H-bridge, built with IRF540N MOSFETs, alternates the polarity of the stepped voltages to obtain the seven-level output. The switching sequence is generated using an Arduino UNO microcontroller is programmed with PWM logic. The control algorithm is designed to ensure that only the certain number of switches operate at each step, thereby reducing conduction and switching losses. Optical isolation and gate

amplification are provided by TLP250 gate drivers powered by isolated 15 V supplies [2, 9, 10].

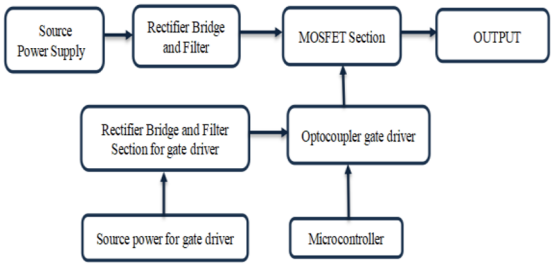

Fig. 1. The block diagram of the 7-Level MLI is given

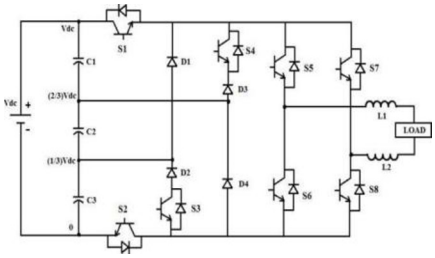

Fig. 2. Circuit Diagram of 7L MLI.

3.1 Modes-O-Operation

For an input voltage Vi, the inverter generates 7 output voltage levels: 0, ±⅓Vi, ±⅔Vi, and ±Vi. The switching sequence is controlled as follows.

- For +⅓Vi, Q1, Q5, and Q8 switches are on, draws voltage from C1.
- For +⅔Vi: Q1, Q4, Q5, Q8 switches are on, draws voltage from C1+C2.
- For +Vi: Q1, Q2, Q5, Q8 switches are on, draws voltage from C1+C2+C3.
- For –⅓Vi: Q2, Q6, Q7 switches are on, draws voltage from C1+C2+C3.
- For –⅔Vi: Q2, Q3, Q6, Q7 switches are on, draws voltage from C2+C3.
- For –Vi: Switch Q2, Q1, Q6, Q7 are on, draws voltage from C1+C2+C3.
- 0: Switch Q5 and Q7 are on , giving zero output.

This switching sequence ensures t h e proper synthesis of voltage while minimizing the device stress [1, 9].

3.1.1 Reduction in Switch Count

In a traditional cascaded -H-Bridge 7L MLI, The total of 12 switches and requires multiple-isolated DC sources. The proposed reduced-switch design achieves the same seven output levels using eight switches and single DC source along with a voltage divider network. This method not only simplifies the control strategy but also reduces:

- Switching losses (fewer transitions per cycle),
- Power device stress, enhancing efficiency and reliability [1, 2, 9].

Table 1. The switching combinations o obtain the seven output voltage levels of the Inverter.

	0	1	2	3	2	1	0	1	2	3	2	1
S1	00	1	1	1	1	1	00	00	00	1	00	00
S2	00	00	00	1	00	00	00	1	1	1	1	1
S3	00	00	00	00	00	00	00	00	1	00	00	00
S4	00	00	1	00	1	00	00	00	00	00	00	00
S5	1	1	1	1	1	1	1	00	00	00	00	00
S6	1	00	00	00	00	00	00	1	1	1	1	1
S7	00	00	00	00	00	00	1	1	1	1	1	1
S8	00	1	1	1	1	1	00	00	00	00	00	00

Calculation of time

Total switching sequence 12

50 Hz time is 1 sec as per 50HZ required 1 cycle time = 1 sec / 50 = 20 millisecond

20 millisecond to micro sec = 20 * 1000=20000 So Total delay in one cycle is 20000 microsecond

In each switching time required 20000/ 12= 1666 Time delay

4 Simulation and Result

The system was simulated in MATLAB/Simulink to validate its performance prior to hardware testing The simulated output exhibited seven distinct voltage steps, forming a waveform that closely resembled a sinusoid. The staircase output demonstrated effective harmonic suppression with reduced THD compared to a conventional two-level inverter. The simulated THD was observed to be in the range of 8–10%, confirming the suitability of the topology for low- frequency applications [4].

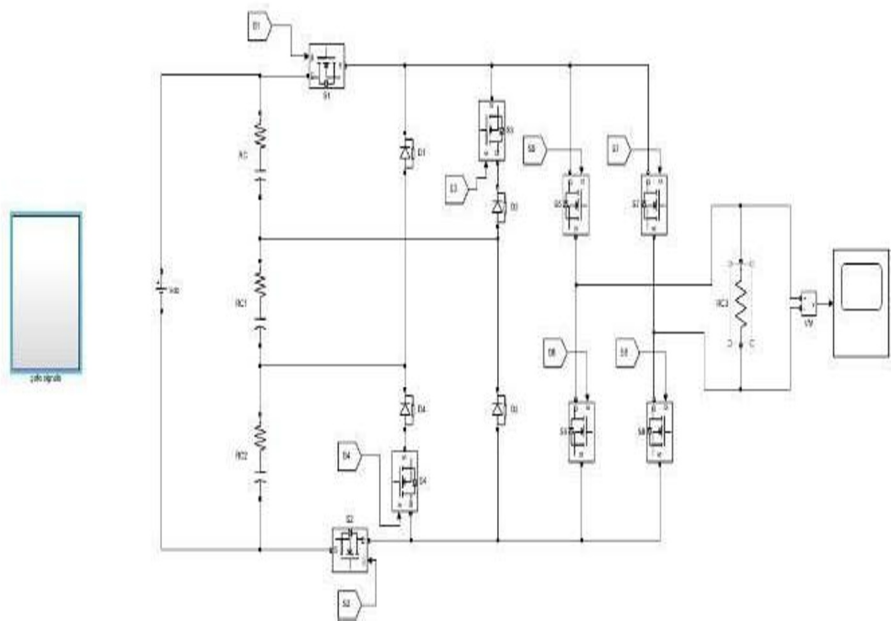

Fig. 3. Simulation view of 7L MLI.

Table 2. The parameters for the proposed 7L MLI.

Parameter	**Value**
Simulation Tool	MATLAB/Simulink
DC Input Voltage (Vi)	30 V
Output Levels	7 (±Vi, ±2/3Vi, ±1/3Vi, 0)
Switching Frequency	50 Hz
Load	R = 100 Ω
Capacitor Values	470 µF each (voltage divider)
Power Devices	MOSFET (IRF540N model)
Gate Driver	TLP250 model
Control Technique	Arduino-based PWM (simulated)

5 Experiment and analysis

To verify the proposed reduced-switch 7-level multilevel inverter (7L-RSMLI), a prototype was constructed using discrete semiconductor devices, an opto-isolated gate driver, and a microcontroller-based control unit. The MOSFETs form the main power stage, while TLP250 driver circuits provide level shifting, optical isolation, and gate amplification. The Arduino UNO (ATmega328P) generates the required switching sequence through programmed PWM signals. A regulated 15 V isolated DC supply is used for the driver circuit, while the control platform operates at 5 V. The DC-link capacitors are connected in series to form a voltage divider that generates stepped input voltages for the H-bridge stage. For initial validation, a purely resistive load was employed, and the output waveform was recorded using a digital oscilloscope. The complete hardware specifications of the prototype are summarized [7, 8].

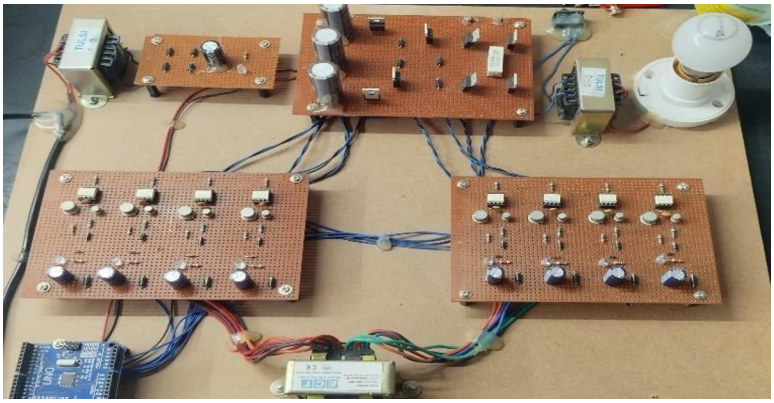

Fig. 5. Hardware implementation.

Table 3. The hardware parameters for the proposed 7L MLI.

Input DC Supply	30–36 V
Driver Supply	15 V DC (isolated)
Capacitors	3 × 470 µF / 50 V (voltage divider)
Diodes	1N4007, 1000 V, 1 A
Load	R = 100 Ω, 50–100 W
Switching Frequency	50 Hz (12 steps, 1666 µs delay)

The following hardware results present the stepped output voltages generated by the inverter. These waveforms confirm that the hardware closely follows the simulated response, producing all seven voltage levels (±Vi, ±2/3Vi, ±1/3Vi, and 0) with acceptable harmonic content. The comparison between hardware and simulation validates the effectiveness of the proposed design.

Fig. 6. The output obtained in CRO with RL Load.

Fig. 7. The output obtained in CRO without RL Load

Table 4. Comparison of Proposed and Conventional Inverters.

Parameter	**Conventional 7L Cascaded H-Bridge**	**Proposed 7L Reduced-Switch MLI**
Number of Switches	12	8
Number of Gate Drivers	12	8
DC Sources Required	3 isolated	1 (with capacitors)
Switching Losses	High	Reduced
Control Complexity	Moderate	Low (Arduino PWM)
Output Voltage Levels	7	7
THD (%)	14–16	8–10
Hardware Cost	Higher	Lower

6 Comparitive Study

The comparison highlights that the proposed system requires less number switches and gate drivers, uses only a single DC source, and achieves lower THD compared to the conventional cascaded H- bridge topology. This results in reduced hardware cost and simplified control implementation [3, 9, 10].

7 Conclusion

A reduced switch 7 level multilevel inverter has been designed simulated, and implemented. The proposed configuration uses only eight switches and one DC source with voltage divider capacitors, thereby lowering hardware complexity and cost Simulation and hardware verification established that the topology produced a staircase sinusoidal output, achieving 8–10% THD reduction compared to conventional models. The inverter is suitable for applications such as standalone converters and motor drives, and future work can extend the. motor drives, and future work can extend the concept to renewable energy system and higher power levels.

References

1. N. V. Mishra, Analysis of multilevel inverter using reduced switch count for harmonic suppression. Int. J. Creative Res. Thoughts (IJCRT) **6**(2), 1205–1210 (2023).
2. M. Chen, Y. Yang, P. C. Loh, F. Blaabjerg, Low-switch-count nine-level boost inverter with single DC source. IEEE Trans. Ind. Electron. **69**(3), 2644–2658 (2023).
3. J. M. Kharade, Study and simulation of cascaded H-bridge based multilevel inverters. Int. J. Innov. Res. Sci. Eng. Technol. **7**(3), 1002–1007 (2022).
4. A. K. Ranjan, Evaluation of PWM strategies for multilevel inverters. In Proc. Int. Conf. Circuit, Power and Computing Technologies (ICCPCT), 1–6 (2022).
5. W. M. Utomo, A. Afarulrazi, SPWM-based modeling of a seven-level cascaded H-bridge inverter for THD minimization. Int. J. Eng. Technol. **7**(2.6), 327–330 (2021).
6. A. Nabae, I. Takahashi, H. Akagi, Neutral-point clamped PWM inverter: A novel topology. IEEE Trans. Ind. Appl. IA-**17**(5), 518–523 (2021).
7. Vishay Siliconix, IRF540N HEXFET® power MOSFET datasheet. Vishay Intertechnology (2020).
8. Arduino, Technical specifications of Arduino UNO Rev3. Arduino.cc (2023).
9. M. D. Siddique, S. Mekhilef, N. M. Shah, M. A. Memon, F. Blaabjerg, Seven-level single-source boost inverter with minimized switch count. IEEE Trans. Circuits Syst. II: Express Briefs **67**(12), 3252–3256 (2020).
10. M. J. Sathik, N. Sandeep, D. Almakhles, F. Blaabjerg, Compact switched-capacitor based multilevel inverter with reduced component count. IEEE Trans. Circuits Syst. II: Express Briefs **67**(12), 3287–3291 (2020).
11. W. Peng, Q. Ni, X. Qiu, Y. Ye, Self-balanced seven-level switched-capacitor inverter and its cascaded structure. IEEE Trans. Power Electron. **34**(12), 11889–11896 (2019).
12. A. Taghvaie, J. Adabi, M. Rezanejad, Step-up multilevel inverter operation with single DC supply. IEEE Trans. Ind. Electron. **63**(12), 6643–6652 (2016).