A study on propagation delay and power dissipation of a 2-bit CMOS magnitude comparator with critical path evaluation

Tirunagari Manudeep [1], *Tirunagari* Manusree [1], *Padilam Adithya Taran* Yadav [1], *Samana* Nagendran [1], *Arjun Sunil* Rao [1*] *and Jennifer Charlotte* Saldanha [2]

[1]Manipal Institute of Technology (MIT), Manipal Academy of Higher Education (MAHE) Manipal, Udupi, India-576104
[2]A.J. Institute of Engineering and Technology Mangaluru, Karnataka, India

Abstract. This work presents the design of 2-bit magnitude comparator in Cadence Virtuoso tool using gpdk090 technology. The detailed analysis of propagation delay and power dissipation (both dynamic and static power) for its outputs—L (A < B), E (A = B), and G (A > B) are analysed. The comparator was simulated and evaluated to quantify delay and power behaviour under varying conditions. Results show that the L (A<B) output achieves the shortest propagation delay of 7.55 ns, while the E (A=B) and G (A>B) outputs incur higher delays of 74.99 ns and 49.20 ns due to longer critical paths. Further, Results reveal that the L (A<B) output achieves the lowest power dissipation, with dynamic and static values of 5.07 mW and 1.49 µW, respectively, owing to its simple hierarchical decision path. The E (A=B) output exhibits the highest dynamic power consumption of 50.51 mW while maintaining a low static dissipation of 1.55 µW. This large dynamic overhead is attributed to the cascaded XNOR and AND logic used in equality detection, which introduces high switching activity and glitching effects. The G (A>B) output demonstrates moderate dynamic power of 8.11 mW but records the highest static leakage of 3.92 µW, arising from device sizing and threshold voltage trade-offs to enhance timing performance. These findings establish that equality detection is the most energy-intensive operation, while greater-than logic suffers from elevated leakage currents. The study provides critical insights into the relationship between logic structure and power characteristics, offering guidance for targeted low-power design strategies in comparator circuits and similar digital building blocks.

1 Introduction

The ongoing growth of wireless technologies, which need a finite supply of power, has increased the demand for VLSI circuits with the least propagation delay [1]. In modern digital circuits, propagation delay is becoming a significant problem. Therefore, the primary goal of VLSI designers is to minimize the propagation delay. In fact, the inverter serves as the foundation of all digital designs [2]. Developing more complex CMOS structures after their function and features is thoroughly understood. A major challenge in the creation of high-

* Corresponding author: arjun.rao@manipal.edu

performance integrated circuits is the generation, distribution, and delay in propagation of the signal. In paper [4], the author presents several low power and high-speed integrated circuit design strategies such as substrate biasing. This technique is used for reducing device power consumption without compromising the speed of the device. The development of semiconductor technology is mostly constrained by the propagation delay [5].

Since propagation delay is one of the most crucial performance factors in CMOS digital circuits, it takes a lot of effort to generate accurate, analytical formulas for timing models of simple circuits. In terms of calculation time and storage costs, using transistor level simulators that represent the devices in continuous time, such as SPICE, can be highly costly [6]. As a result, a large portion of previous research has focused on creating analytical delay models without the need for costly numerical iterations. As designs approach the complexity of the gates, gate level safety characterization in the design space is required to preserve a temporal relationship between functional blocks [7]. Much work has been done to develop accurate and useful models in the cadence libraries involving CMOS level transistor circuits. Controlling or guiding design options, technology migration, and process evolution all depend on these models. They are used to assess the performance of certain structures. In conventional two-term delay modelling, a constant "inertial" characteristic of delay in the cell is connected to an output-load related delay characteristic of the cell's size and structure. Regarding overestimated process dispersion, this representation might assist designers in concentrating their design performances. In the submicron range where second-order effects take centre stage, this seems to be insufficient. As is frequently seen, nonlinearity for the propagation delays is caused by coupling effects of inputs and outputs linked to the carriers' speed saturation. These effects are sufficiently important to warrant consideration in a rigorous standard cell-delay performance evaluation [8]. So, by switching the circuit design the delay in gate influences operation, and surroundings in addition to the input-switching signal's wave shape, which is typically defined as the time it takes for controlling gate's output and voltage to change between suitable voltage levels. The delay is also significantly influenced by these signal rise and fall durations, which causes nonlinear change in the actual delay values. Consequently, it becomes essential to describe gate delay while accounting for output-transition durations and propagation [9].

This research focusses on the simulation of CMOS 2-bit magnitude comparator circuit. This circuit consists of two inputs A and B, two bits each, whose magnitudes are to be compared and three outputs viz. "(A<B)", "A=B" and "A>B". These outputs correspond to L, E, and G conditions, respectively. The static CMOS logic is used to implement the circuit. The propagation delay and the dynamic power dissipation of the three outputs are studied. The simulation of these circuits was conducted using Cadence Virtuoso simulation tool.

2 Methodology

2.1 Simulation framework

Cadence Virtuoso is an EDA (Electronic Design Automation) application that can handle practically every area of layout design, experimental simulation, electronic design, and more. Mentor Graphics, Synopsys, and other software packages offer similar features. However, compared to competing EDA tools, Cadence Virtuoso provides more sophisticated capabilities for circuit modelling, circuit diagram design, layout design, and wiring. Cadence also develops a simulation process library and shares data with other semiconductor companies, making simulation easier for consumers. The process flow for conduction of this research work is based on the flowchart illustrated in Fig. 1.

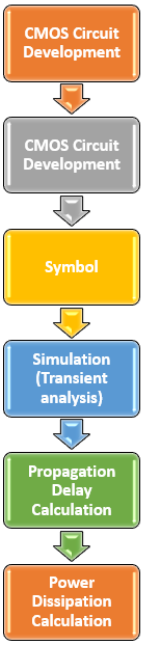


Fig. 1. Process flow for simulation used in this research.

In terms of the process flow, initially the schematic of the static CMOS 2-bit magnitude comparator circuit was designed. Two 2-bit inputs, A and B, and three 1-bit outputs "Less than" i.e. L (A<B), "Equal to" i.e. E (A=B) and "Greater than" i.e. G (A>B), make the 2-bit magnitude comparator circuit. Using this schematic, the symbol is created and required voltage sources are connected to the inputs and V_{DD} creating the test circuit. This test circuit is used to do two types of studies, i.e. the circuit's propagation latency and dynamic power dissipation. Propagation delay can be defined as the time taken by the circuit to reach from input to output of any VLSI circuits. Because it influences the circuit's overall speed and performance, this delay is a crucial design element for digital circuits. As the input signal varies, short circuit (direct path) currents between the pMOS and nMOS transistors cause dynamic power, as do switching currents needed to charge and discharge output loads.

2.2 Design of 2-bit magnitude comparator circuit

A digital circuit known as 2-bit magnitude comparator is used to compare two 2-bit binary integers, usually denoted A and B. It determines the relationship between the two numbers, providing three possible outputs. The 2-bit magnitude comparator truth table is shown in Table 1. By analysing the truth table of 2-bit magnitude comparator the Boolean expressions for the outputs L (A<B), E (A=B) and G (A>B) are obtained as Equations (1), (2) and (3), respectively.

$$L\ (A < B) = \overline{A_1}B_1 + \overline{A_1}\ \overline{A_0}B_0 + \overline{A_0}B_1B_0 \quad (1)$$

$$E\ (A = B) = \overline{(A_0 \oplus B_0)}\ \cdot \overline{(A_1 \oplus B_1)} \quad (2)$$

$$G\ (A > B) = A_1\overline{B_1} + A_0\overline{B_1}\ \overline{B_0} + A_1A_0\overline{B_0} \quad (3)$$

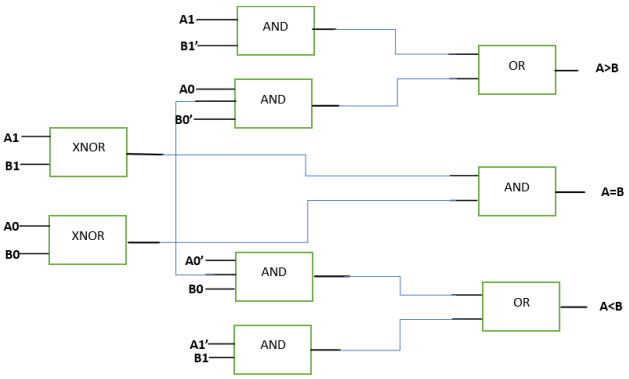
Table 1. Truth table of 2-bit magnitude comparator.

Input A		Input B		Outputs		
A_1	A_0	B_1	B_0	L $(A<B)$	E $(A=B)$	G $(A>B)$
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

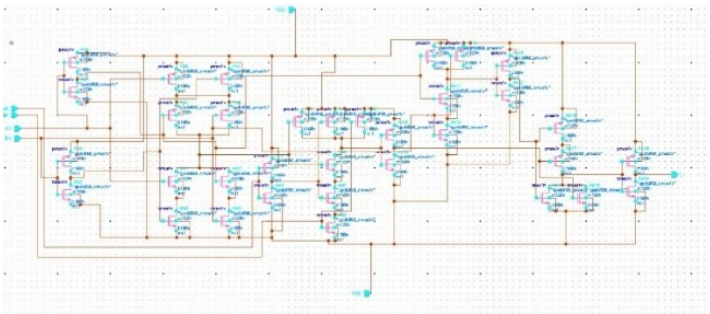
Cadence Virtuoso tool has been used to construct a static CMOS circuit of the 2-bit magnitude comparator based on these Boolean expressions to investigate the outputs' propagation delay and dynamic power dissipation. A pMOS transistor array in pull-up network (PUN) and a nMOS transistor array in pull-down network (PDN) make up static CMOS circuits, which are the basic building block of VLSI design. The configuration of these PDN and PUN is complimentary. The block diagram for implementation of 2-bit comparator, is shown in Fig. 2(a). The schematic circuits for L (A<B), E (A=B), and G (A>B) are shown in Figs. 2(b), 2(c) and 2(d), respectively. The parameters of transistor sizing are illustrated in Table 2.

2.3 Symbol of 2-bit magnitude comparator circuit

The 2-bit magnitude comparator circuit schematic gets transformed into a symbol. A schematic can be represented as a single block in Cadence Virtuoso by creating a symbol, which facilitates integration into bigger circuits. The necessary analysis was carried out using the generated symbols as test circuits. Fig. 3 displays the 2-bit magnitude comparator circuit symbol which is used to compute dynamic power dissipation and propagation delay. Table 3 provides a summary of the input signals A and B's parameters.



(a)



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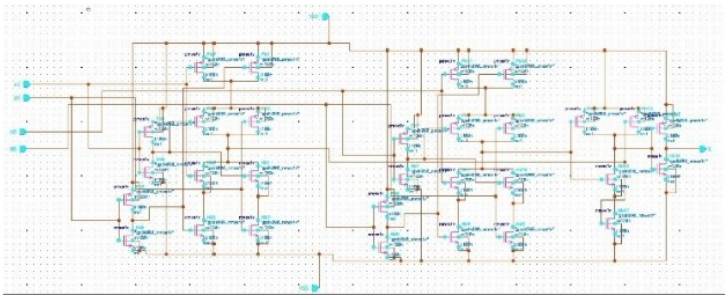
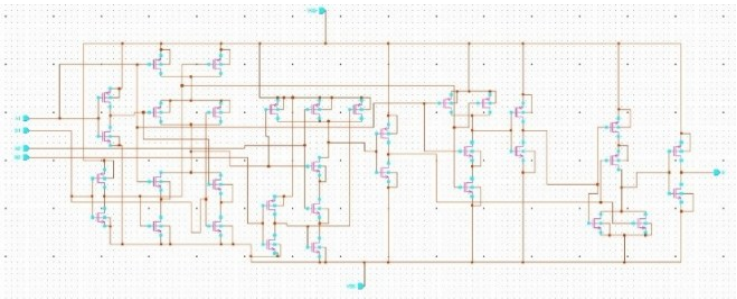


(c)



(d)

Fig. 2. CMOS logic implementation of 2-bit comparator circuit showing, (a) block diagram, and schematic circuit of, (b) L (A<B), (c) E (A=B), and (d) G (A>B).

2.4 Propagation delay and power dissipation

The propagation delay and dynamic power dissipation of static CMOS comparator circuits are the main subjects of this work. Propagation delay can be defined as the time taken by the circuit to reach from input to output in CMOS circuits. This delay plays a vital role in digital circuit design since it affects the circuit's overall speed and performance. The propagation delay was calculated from the transient response of circuits. Dynamic power dissipation is the power consumed when a CMOS circuit switches states due to charging and discharging of load capacitances during input transitions. Static power dissipation is the power consumed when the circuit is idle, mainly caused by leakage currents through transistors. Together, they determine the total power consumption, with dynamic dominating in active mode and static becoming significant in scaled technologies.

Table 2. Details of pMOS and nMOS widths. The lengths of all transistors are 90 nm.

Circuit	Number of inputs	Width of nMOS (nm)	Width of pMOS (nm)
AND	3	360	240
	2	240	240
OR	3	120	720
	2	120	480
Inverter	1	120	240

Table 3. Summary of voltage sources used in designing of 2-bit magnitude comparator circuit.

Parameters	Input A1	Input A0	Input B1	Input B0
Voltage 1 (V)	0	0	0	0
Voltage 2 (V)	1.8	1.8	1.8	1.8
Period (ns)	30	20	40	25
Delay time (ns)	10	10	15	10
Rise and fall time (fs)	1	1	1	1
Pulse width (ns)	15	10	20	10

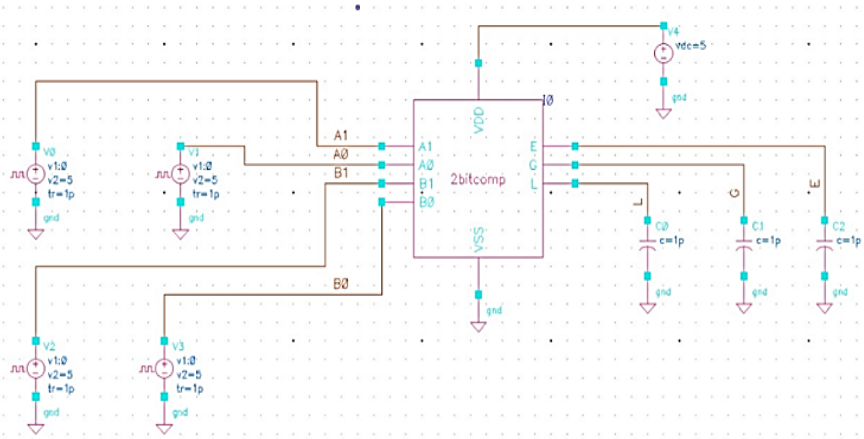


Fig. 3. Symbol of CMOS 2-bit magnitude comparator circuit generated from the schematic.

3 Results And Discussions

This paper's primary goal is to analyse the intended configuration, design, and symbol of a CMOS 2-bit comparator circuit. In this study, propagation delay and power dissipation and are considered as features, and the best functionality among the others is finally identified.

3.1 Propagation delay

Delay can be calculated starting when the input reaches half, or 50 % of the supply power, and when the output likewise has a comparable voltage, as shown in Fig. 4. For the high-to-low and low-to-high transitions in the output, determine the input-to-output signal delay for the propagation delay periods τ_{PHL} and τ_{PLH}, respectively. The time needed for the output voltage to drop from V_{OH} to the $V_{50\%}$ level is known as the τ_{PHL}, while the time needed for the output voltage to increase from V_{OL} to the $V_{50\%}$ level is known as the τ_{PLH}. In Equation (4), the voltage points $V_{50\%}$ are defined [10]:

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH}) \quad (4)$$

Consequently, the propagation delay times τ_{PHL} and τ_{PLH} are taken from Fig. 4 as Equations (5) and (6), respectively. The average propagation delay (τ_P) is given by Equation (7) as, :

$$\tau_{PLH} = b - a \quad (5)$$

$$\tau_{PHL} = d - c \quad (6)$$

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \quad (7)$$

Where, a is the time when input falls and crosses $V_{50\%}$, b is the time when output rises and reaches $V_{50\%}$, c is the time when input rises and crosses $V_{50\%}$, and d is the time when output falls and reaches $V_{50\%}$.

Fig. 4. Calculation of propagation delay.

Fig. 5 shows the designed static CMOS 2-bit comparator circuit's simulated input and output waveforms. For each possible combination, the inputs (A and B) are applied to simulated waveforms, i.e., 00, 01, 10 and 11. The supply voltages used to mimic the circuits vary from 0 to 1.8 V, which correspond to logic 0 and logic 1, respectively. For the circuit that was designed, the supply voltage (V_{DD}) is 1.8V. The variation of τ_{PHL}, τ_{PLH} and τ_P for CMOS 2-bit magnitude comparator circuit are summarized in Table 4.

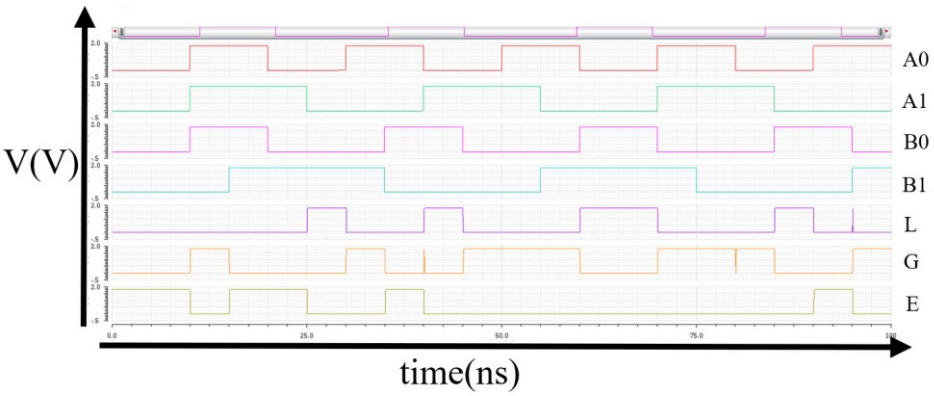


Fig. 5. Simulated input and output waveforms of the designed CMOS 2-bit magnitude comparator circuit.

Table 4. Summary of propagation delay for CMOS 2-bit magnitude comparator circuit

Outputs	Time delay		
	Falling delay, τ_{PHL}	Rising delay, τ_{PLH}	Propagation delay, τ_P
L (A<B)	61.03 ps	15.05 ns	7.55 ns
E (A=B)	4.90 ns	5.06 ns	74.99 ns
G (A>B)	9.95 ns	4.93 ns	49.20 ns

In a 2-bit magnitude comparator, the outputs L (A < B), E (A = B), and G (A > B) are generated by evaluating the relationship between two 2-bit binary numbers. Each of these outputs is implemented through different logical structures, and hence, the signal propagation delays vary depending on the number of logic levels, the critical path of signal flow, and the nature of transitions (falling or rising). Table 4 indicates the measured falling delay (τ_{PHL}), rising delay (τ_{PLH}), and overall propagation delay (τ_P) for the three outputs. Analysing these results in the context of comparator design provides useful insights into the delay behaviour of digital circuits.

For the L (less than) output, the falling delay is extremely small at around 61.03 ps, which is negligible compared to its rising delay of 15.05 ns. This suggests that the logic path for a falling transition in L (A<B) is much shorter and encounters fewer gate delays than that for a rising transition. The propagation delay, reported as 7.55 ns, lies between these two values, implying that the average delay is still within the nanosecond range and relatively small compared to the other outputs. In a magnitude comparator, the L (A<B) output typically depends on the most significant bit (MSB) first, and only if those are equal, does the comparator evaluate the lower bits. This hierarchical evaluation leads to certain paths having very fast switching for one transition direction while others take longer, which is evident in the sharp difference between τ_{PHL} and τ_{PLH}. Overall, the L (A<B) output shows moderate delay behaviour, but with strong asymmetry between rising and falling transitions. The E (equal to) output shows a very different behaviour. Both the falling and rising delays are close in value, 4.90 ns and 5.06 ns, respectively. This indicates that the logic for equal comparison is fairly balanced in terms of its switching activity, and neither the high-to-low nor low-to-high transition dominates. However, the reported propagation delay is 74.99 ns, which is much larger than the expected average (~5 ns). This discrepancy suggests that for the equal output, τ_P is not computed as the average of the rising and falling delays but rather as the worst-case critical path delay through the comparator circuit. The equality condition requires that every bit of A and B be compared and verified as identical. This often involves cascaded XNOR gates and an AND gate combining all equality results, creating a longer critical path. Even if the gate-level delays for individual transitions are small, the complete evaluation of equality can stretch the worst-case propagation time. Hence, τ_P for E (A=B) is disproportionately high, reflecting the extensive logic path involved in generating this output. For the G (greater than) output, the falling delay is 9.95 ns, while the rising delay is slightly smaller at 4.93 ns, indicating that the circuit is somewhat asymmetric in its transition responses but not as extreme as in the L (A<B) output. The propagation delay is given as 49.20 ns, which, like in the case of E (A=B), is much higher than the simple average of τ_{PHL} and τ_{PLH}. This again points to the consideration of the worst-case delay path in reporting τ_P. In comparator circuits, the G (A>B) output is typically determined first by the MSB, similar to the L (A<B) output, but when the MSBs are equal, the logic must extend into the lower-order bits, thereby increasing delay. Since the determination of "greater than" involves multiple conditional checks and priority logic, the worst-case propagation delay for G (A>B) becomes significantly higher than its immediate rising or falling delays.

In summary, the delay analysis of the 2-bit magnitude comparator highlights how the structure of logic for each output impacts the timing behaviour. The L (A<B) output demonstrates very fast falling transitions but comparatively slower rising ones, giving a

moderate propagation delay overall. The E (A=B) output, though balanced in individual rising and falling transitions, suffers from an extremely high propagation delay due to the need for a complete bit-wise equality check across all inputs, which creates a long critical path. The G (A>B) output lies between the two extremes, with moderate individual transition delays but still a large propagation delay caused by hierarchical decision-making logic. These results underline an important principle of digital design: propagation delay is not always a simple average of transition delays but is heavily influenced by the critical path length, logic depth, and evaluation conditions unique to each output in a circuit.

3.2 Dynamic and static power dissipation

When analysing the power dissipation characteristics of a 2-bit magnitude comparator, it is important to distinguish between the two fundamental components of power consumption in digital CMOS circuits: dynamic power dissipation and static power dissipation. Dynamic power arises primarily from the charging and discharging of load capacitances during logic transitions and is strongly dependent on the switching activity of the circuit, the capacitive load, the supply voltage, and the operating frequency. Static power, on the other hand, corresponds to leakage currents that flow even when the circuit is not switching, and it is generally determined by device-level parameters such as threshold voltage, transistor sizing, and bias conditions. The results obtained for the comparator show distinct behaviours across the three outputs—L (A < B), E (A = B), and G (A > B)—reflecting the influence of logic complexity, signal activity, and transistor-level implementation on power consumption. Figs. 6,7 and 8 show the dynamic power dissipation of 2-bit magnitude comparator circuit for the outputs L (A<B), E (A=B), and G (A>B), respectively. Table 5 summarizes the dynamic and static power dissipation for all the three outputs.

For the L (A < B) output, the dynamic power dissipation is measured to be 5.07 mW, which is the lowest among the three outputs. This indicates that the less-than logic is relatively simple in structure and involves fewer active switching nodes. In a typical comparator, the "less than" output can often be resolved quickly by examining the MSB of the inputs, and only when the higher-order bits are equal does the circuit evaluate the lower-order bit. This early-exit mechanism reduces unnecessary switching, resulting in low effective switching activity and, consequently, lower dynamic power. The static power dissipation for L (A<B) is found to be 1.49 μW, which is also small. This suggests that the L (A<B) logic network is implemented with either smaller transistors or more stacked devices, which suppress leakage currents through the stack effect. Together, these results highlight that the L (A<B) path in a 2-bit comparator is energy-efficient, with both dynamic and static contributions kept minimal due to its shorter logic path and limited switching activity. The E (A=B) output demonstrates a drastically different behaviour, with a dynamic power dissipation of 50.51 mW, which is nearly an order of magnitude higher than both L (A<B) and G (A>B) outputs. The equality condition in a comparator is inherently more complex, as it requires verification that all corresponding input bits are identical. This is typically implemented using cascaded XNOR gates followed by an AND operation to combine the results of bitwise comparisons. Such a configuration not only involves a larger number of internal nodes but also increases the likelihood of glitching, where transient logic transitions occur due to mismatched arrival times of input signals. These glitches contribute to excess charging and discharging of internal capacitances, thereby significantly elevating the dynamic power dissipation. Interestingly, the static power for the E (A=B) output is reported as 1.55 μW, which is nearly the same as that of the L (A<B) output. This indicates that the excessive power overhead of the E (A=B) path is not due to leakage but almost entirely due to dynamic switching. This observation emphasizes that the equality logic in comparators is a critical contributor to overall energy inefficiency, and hence design optimizations such as path balancing, glitch reduction techniques, or operand isolation could be particularly beneficial in reducing its dynamic power footprint. The G (A > B) output lies between the two extremes, exhibiting a

dynamic power dissipation of 8.11 mW, which is higher than L (A<B) but substantially lower than E (A=B). This suggests that the greater-than logic has a moderate logic depth and switching activity. Like the L (A<B) output, the G (A>B) decision is often determined first by evaluating the MSB, and further evaluation only occurs if the MSBs are equal. Therefore, although the logic activity is higher than that of L (A<B), it is still limited compared to the equality output. The most notable characteristic of the G (A>B) output is its static power dissipation of 3.92 μW, the highest among all three outputs. This elevated leakage indicates that the G (A>B) path may have been implemented using larger transistors or lower-threshold devices to meet timing requirements. Wider transistors reduce resistance and speed up critical transitions but simultaneously increase leakage due to greater subthreshold and gate oxide currents. Moreover, a smaller degree of stacking in the transistor network can also lead to higher leakage, as fewer devices in series are available to suppress the current in standby mode. Thus, while the G (A>B) output is not as dynamically costly as the E (A=B) output, its static power dissipation represents an important concern for low-power design.

Overall, the results reveal distinct power dissipation profiles for each comparator output, underscoring the trade-offs between logic complexity, timing requirements, and energy efficiency. The E (A=B) output is dominated by dynamic power consumption due to its structurally complex equality-checking logic, the L (A<B) output achieves the lowest overall power dissipation owing to its simple and efficient decision path, and the G (A>B) output exhibits moderate dynamic consumption but the highest static leakage, likely due to design choices prioritizing speed. These findings highlight the importance of targeted optimization strategies: glitch reduction and capacitance minimization for the equality logic, leakage control techniques such as multi-threshold devices or transistor stacking for the greater-than logic, and maintenance of efficient early-exit structures for the less-than logic. For journal-level discussion, these insights demonstrate how architectural and circuit-level decisions manifest in measurable power differences, thereby providing a basis for proposing design modifications aimed at reducing the energy footprint of comparator circuits.

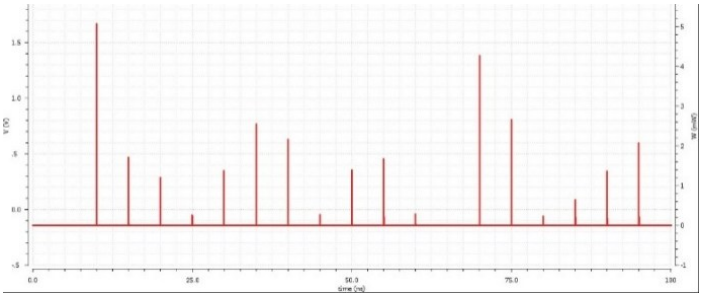


Fig. 6. Dynamic power dissipation for the output L (A<B).

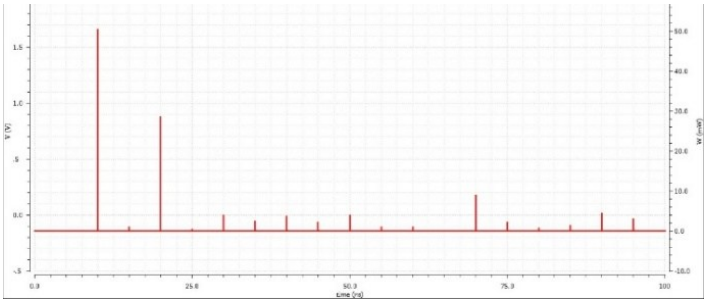


Fig. 7. Dynamic power dissipation for the output E (A=B).

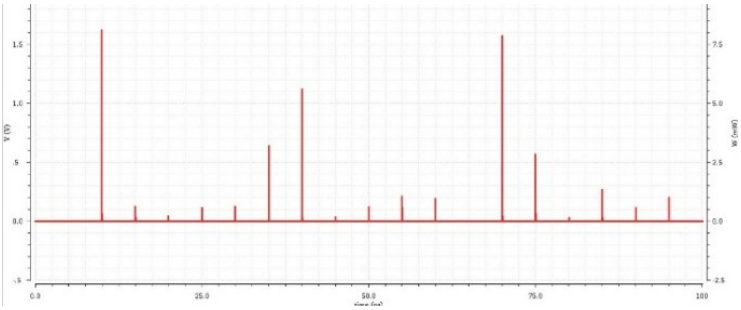


Fig. 8. Dynamic power dissipation for the output G (A>B).

Table 5. Summary of dynamic and static power dissipation for CMOS 2-bit magnitude comparator circuit.

Outputs	Dynamic power dissipation (mW)	Static power dissipation (µm)
L (A<B)	5.07	1.49
E (A=B)	50.51	1.55
G (A>B)	8.11	3.92

4 Conclusions

In this work, the propagation delay and power dissipation characteristics of a 2-bit magnitude comparator were comprehensively analysed with respect to its three outputs: L (A < B), E (A = B), and G (A > B). The L (A < B) output exhibits the shortest overall propagation delay of 7.55 ns, attributed to its relatively simple hierarchical evaluation path and minimal logic depth. In contrast, the E (A = B) output incurs the largest delay of 74.99 ns, despite having nearly balanced rising (5.06 ns) and falling (4.90 ns) transition times. This significant delay overhead arises from the cascaded XNOR and AND gate structure required for equality detection, which introduces a longer critical path. The G (A > B) output shows an intermediate propagation delay of 49.20 ns, with rising and falling delays of approximately 5–10 ns. This moderate performance reflects a trade-off between logic complexity and signal evaluation depth. Overall, the results indicate that equality detection is the most timing-critical operation in the comparator, while the less-than condition is resolved fastest. Further, the study demonstrated that the power consumption profile of each output is strongly influenced by the underlying logic complexity and circuit structure. The L output exhibited the lowest overall power consumption, with both dynamic and static contributions remaining minimal due to its efficient hierarchical evaluation path. In contrast, the E output showed significantly higher dynamic power dissipation, which can be attributed to the cascaded XNOR and AND logic required for equality detection, leading to increased switching activity and glitching. The G output displayed moderate dynamic power but recorded the highest static power dissipation, a consequence of transistor sizing and threshold trade-offs that reduce delay but increase leakage. These findings highlight the inherent trade-offs in comparator design, where equality checking is the most dynamic-power-intensive operation, and greater-than logic is more susceptible to leakage. The results suggest that targeted optimization strategies are essential for low-power comparator implementations. Techniques such as glitch reduction, balanced logic paths, operand isolation, and the use of multi-threshold or power-gated devices could significantly improve the energy efficiency of such

circuits. Beyond comparators, these insights extend to other fundamental arithmetic and decision-making circuits, providing a foundation for designing power-aware digital systems that meet the growing demands of energy-efficient computation.

Acknowledgment

For their helpful support throughout this work, the authors would like to thank Manipal Institute of Technology, Manipal Academy of Higher Education, Manipal.

ORCiD

Arjun Sunil Rao: https://orcid.org/0000-0002-8537-3775

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