The Influence of Interface Modification and Etched SiO_2 Layers on the Photoelectric Performance of Bottom-Contact Organic Field-Effect Transistors (BC-OFETs)

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Abstract. This study proposes a strategy that integrates the collaborative optimization of Etched SiO2 Layers with interface modification, and systematically examines the effects of the etching process, OTS (octadecyltrichlorosilane) modification layer, and PFBT (pentafluorobenzenethiol) modification layer on the performance of bottom-gate-bottom contact (BC-OFET) devices. A continuous planar electrode structure was constructed via 30-second wet etching. In conjunction with OTS/SiO_2 interface modification and PFBT/Cu electrode modification, dual enhancements in carrier transport efficiency and photosensitive characteristics were achieved. The results indicate that: the carrier mobility of the optimized device increased from 1.05×10-3 $cm^2/V·s$ to 6.36×10-3 $cm^2/V·s$ (a 6.06-fold improvement), the threshold voltage decreased from -25V to -16V, the external quantum efficiency (EQE) reached 564.54%, and the photoresponsivity (R) increased to 2.95A/W. The light-dark current ratio reached 2.00. Research demonstrates that the etching structure eliminates the step difference between the electrode and dielectric layers, OTS enhances the quality of semiconductor crystallization, and PFBT improves the matching of electrode work functions.

Keywords: Etching structure; OTS; PFBT; modification; photoelectric sensor

1. Introduction

Organic field-effect transistors (OFETs) have attracted considerable attention for their potential applications in flexible electronics[1], wearable devices[2], and photonic systems[3] due to their inherent flexibility, cost-effective solution processing, and capability for large-area fabrication . Among these, photonic OFETs (PhotOFETs) are particularly promising for advanced functionalities such as light detection, imaging sensors, and artificial vision systems[4]. However, traditional bottom-contact (BC) OFETs face significant challenges[5], including high contact resistance, inefficient carrier injection, and suboptimal interfacial properties[6], which severely limit their photovoltaic performance[7].

The primary challenges in BC-OFETs stem from interfacial defects caused by electrode/semiconductor misalignment and non-uniform semiconductor growth attributed to step-height differences between electrodes and dielectric layers[8]. Recent studies have shown that etched SiO_2 dielectric layers and interface engineering strategies, such as self-assembled monolayers (SAMs), can effectively address these issues. For example, Jeong-Woo Park et al. achieved a mobility enhancement to 1.4 × 10^{-2} $cm^2/V·s$ through the combination of etched SiO_2 and direct Au/polymer contact[9], while Wang et al. improved pentacene-based OFETs by integrating L-cysteine/PEDOT:PSS treatment with etching techniques[10]. Despite these advancements, the optimization of SAM-modified electrodes in conjunction with three-dimensional architectures remains largely unexplored[11].

This study systematically investigates the synergistic effects of etching, OTS-modified SiO_2, and PFBT-functionalized Cu electrodes on the performance of BC-OFETs. The key findings indicate that etched structures eliminate interfacial step-height discrepancies, OTS enhances the crystallinity of pentacene, and PFBT was employed to modify the Cu electrode layer, enabling a better match of the work functions between the organic layer and the metal electrode, resulting in a 6.06-fold improvement in mobility and an external quantum efficiency (EQE) of 564.54%.

2. Experiment

2.1 Materials and Tests

pentacene, OTS, PFBT and chloroform (purity >99%) were purchased from Sigma-Aldrich. All the materials were not further purified and were used directly.All electrical characteristics and photosensitivity of the devices were evaluated under ambient conditions with 650 nm illumination (2–10 mW cm^2) employing a

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Keithley 2636 semiconductor parameter analyzer. The surface morphology of the thin films was characterized through Atomic Force Microscopy (AFM). The internal molecular packing conFigureuration was further examined using a UV-Vis spectrophotometer (Lambda 950).

2.2 Device Preparation

A bottom-gate bottom-contact (BGBC) architecture was employed for the organic field-effect transistor (OFET) fabrication. Figureure 1.a and 1.b illustrates the molecular structure of pentacene, while Figureure 1.c presents the cross-sectional schematic of the OFETs utilizing Cr/Cu bilayer electrodes as source/drain contacts. The device structure comprises heavily doped n-type silicon wafers serving as both substrate and gate electrode, with a 300 nm thermally grown SiO_2 layer acting as the gate dielectric. The fabrication sequence includes: (1) Sequential ultrasonic cleaning of the N-type silicon substrate with acetone, ethanol, and deionized water (10 min each); (2) Patterned channel formation followed by thermal evaporation of 30 nm Cu electrodes through shadow masks; (3) Dielectric surface modification through 2-hour immersion in 1:10 OTS/chloroform solution, subsequent acetone ultrasonic rinsing (30 min); (4) PFBT self-assembled monolayer (SAM) formation via vacuum-assisted deposition - the substrate was inverted above a 1:10 PFBT/ethanol solution in a vacuum chamber, achieving molecular assembly over 12 h through solvent evaporation; (5) Pentacene active layer deposition using thermal evaporation (70 °C substrate temperature, 230 °C source temperature) under high vacuum (<10^{-3} Pa) at 0.5 nm/min rate, yielding 300 nm thick films.

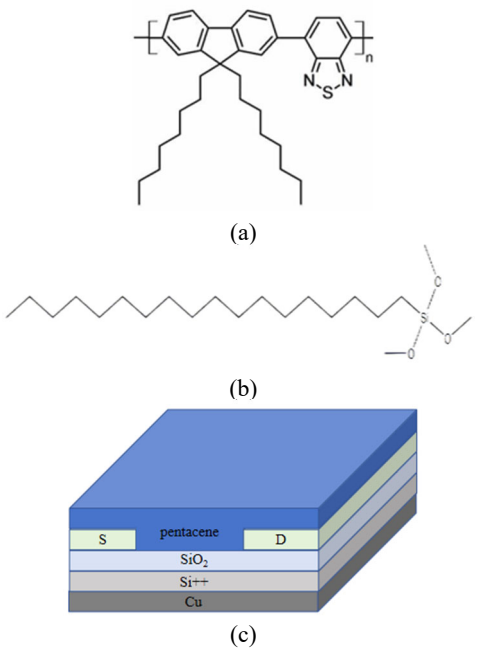
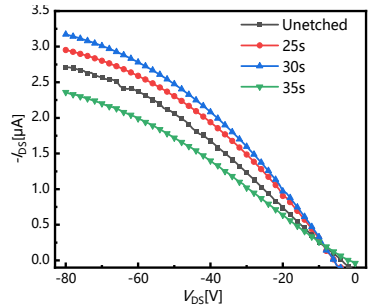


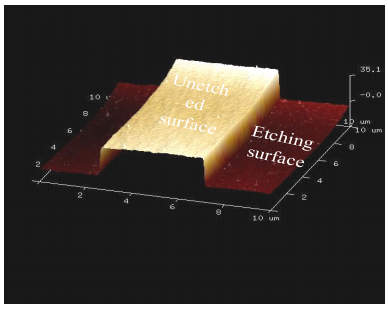
Figure. 1 The molecular structure diagrams of PFBT(a) and OTS(b) and (c) the cross-sectional view of the BC-OFET device

3. Results and Discussion

To address the limited carrier mobility in organic devices, this study employs a bottom-contact (BC-OFET) architecture to maximize probe contact area. A etching process was implemented to optimize the device structure, eliminating step-like interfaces and enhancing the growth continuity of organic films in source/drain regions. As demonstrated in Figureure. 2a, devices etched for 30 s achieved a carrier mobility of 2.19×10^{-3} $cm^2/V\cdot s$, representing a ~100% improvement over non-etched counterparts. Concurrently, the threshold voltage decreased from -25 V to -19 V, and the current on/off ratio increased to 3.02×10^3, indicating superior comprehensive performance compared to control groups with varying etching durations. However, excessive etching (>30 s) led to mobility degradation (1.19×10^{-3} $cm^2/V\cdot s$ at 35 s) and threshold voltage drift (-26 V), attributed to lateral etching-induced interfacial defects in the SiO_2 layer. Atomic force microscopy (AFM) characterization of 30 s-etched samples (Figureure. 2b) revealed precise etching depth control at 30±1 nm, aligning with the total thickness of the adhesion/electrode layers (30 nm) while preserving the 300 nm SiO_2 dielectric layer. This selective etching eliminated interfacial step discrepancies, enabling continuous and ordered growth of organic semiconductor layers in source/drain regions, thereby reducing contact resistance and improving carrier transport efficiency. When the etching time exceeds the material diffusion equilibrium threshold, excessive lateral etching damages the interface flatness, resulting in the deterioration of device performance. These findings confirm that etching optimizes device performance via interfacial engineering.



(a)



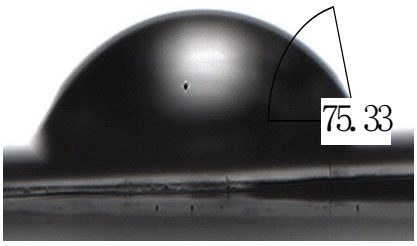
(b)

Figure. 2 (a) Output characteristics curves of OFETs under varying etching durations(b) AFM 3D topography of 30 s-etched specimen

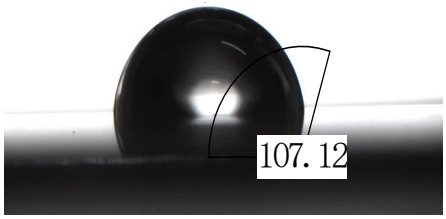
Building upon the previously optimized 30 s etching process (etching depth: 30 nm), this study further employed OTS for chemical modification of the dielectric layer surface and PFBT for self-assembled monolayer (SAMs) modification of Cu electrodes. Water contact angle analysis was conducted to evaluate the hydrophobicity changes at the SiO_2 surface before and after modification (Figure. 3). As shown in Figure. 3(a) and 3(b), the water contact angle of bare SiO_2 increased from 75.33° to 107.12° post-modification. The enhanced hydrophobicity (lower surface energy) facilitates pentacene growth.

As presented in Table 1, the dual-modified device exhibited significant performance improvements in dark conditions: the saturation current density increased to 53.2 μA/cm² (132% enhancement compared to the unmodified device), and the Ion/Ioff ratio surged from 3.02 × 10³ to 1.16 × 10⁴ (284% improvement).

Further quantification via transmission line method (TLPS) (Figure. 4, Table 1) demonstrated that the contact resistance decreased from 9.2 × 10⁵ Ω·cm to 3.55 × 10⁵ Ω·cm (60% reduction) after dual modification. This improvement likely stems from the synergistic effects of SAMs passivating Cu electrode surface oxides and OTS forming a low-defect passivation layer on the dielectric surface, jointly optimizing the interfacial carrier injection barrier [12]

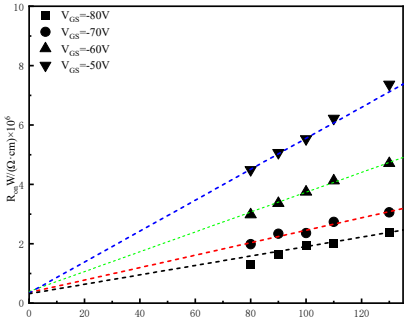


(a)

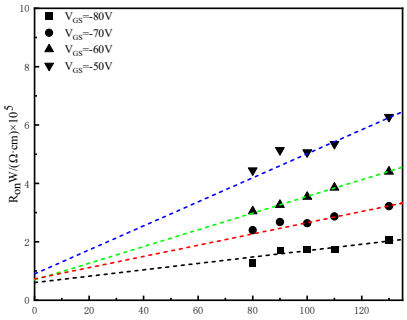


(b)

Figure. 3 (a) schematic diagrams of the water contact angles on the SiO2 surface after unmodified and (b) after OTS modification



(a)



(b)

Figure. 4 Shows the contact resistance of the planar bottom contact structure device when (a) is unmodified and (b) Dual-modified device

Table 1. Electrical Characteristics and Contact Resistance Parameters of the device

Device	I_{sat}(μA)	Mobility ($\times10^{-3}cm^2/V\cdot s$)	V_{th} (V)	I_{on}/I_{off}	R (Ω·cm)
(Unmodified)	17.5	1.05	-25	2.23×10^3	9.2×10^5 Ω·cm
(Modified)	53.2	6.36	-16	$1.16x10^4$	3.55×10^5 Ω·cm

To elucidate the impact of surface modifications on device performance in planar bottom-contact architectures, atomic force microscopy (AFM) was employed to characterize the thin-film morphology of the pentacene active layer. As shown in Figureure. 5, significant differences in pentacene growth morphology were observed at the Cu/SiO_2 interface, Cu electrode surfaces, and SiO_2 dielectric surfaces before and after OTS-PFBT co-modification. Figureure. 5(a) and 5(b) compare the pentacene growth at the Cu/SiO_2 junction in unmodified and modified devices. Prior to OTS-PFBT co-modification, pentacene exhibited smaller crystallites at the Cu/SiO_2 interface. Post-modification, the pentacene morphology at both the Cu electrode and SiO_2 dielectric surfaces showed marked improvement, with surface roughness decreasing from 19 nm (unmodified) to 9.69 nm. Notably, at the Cu/SiO_2 junction, OTS-PFBT co-modification created a continuous transition between pentacene layers grown on Cu electrodes and SiO_2 dielectrics, significantly enhancing carrier injection

efficiency across source/drain electrodes and the organic semiconductor.

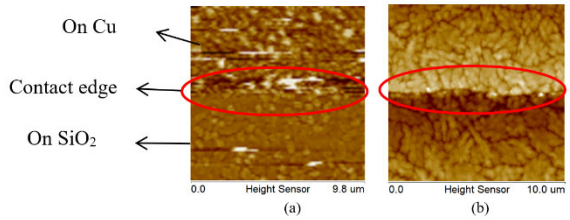


Figure. 5 Atomic force micrographs of pentacene on Cu and SiO2 (Image size = 10 um x 10 um)(a) before modification (b) after modification

Based on the optical absorption characteristics analysis of pentacene thin films (Figureure. 6(a)), four characteristic absorption peaks are observed in the ultraviolet-visible-near-infrared range (543–663 nm), indicating its potential for broad-spectrum photoresponse. In this study, photovoltaic performance testing of OTS/PFBT co-modified planar bottom-contact OFET devices was conducted under 650 nm illumination (10 mW cm^{-2} intensity, Figureure 6(b)). Under dark conditions at a gate voltage of -80 V, the device exhibited a saturation current density of 53 μA cm^{-2}. When illuminated, the saturation current density increased linearly to 160 μA cm^{-2} as the light intensity rose from 0 to 10 mW cm^{-2}, demonstrating significant photoresponse enhancement.

Photovoltaic conversion analysis revealed field-effect mobilities of 6.36×10^{-3} $cm^2/V\cdot s$ (dark) and 16.5×10^{-3} $cm^2/V\cdot s$ (under 10 mW cm^{-2} illumination), corresponding to a 2.6-fold mobility enhancement induced by photoexcitation. Photoresponse characterization (Figureure.6(b)/Table 2) showed that The field-effect mobility of the modified device in the dark state and under 10mW/cm^2 light was 6.36×10^{-3} $cm^2/V\cdot s$ and 16.5×10^{-3} $cm^2/V\cdot s$ respectively, and the mobility caused by light excitation increased by up to 2.6 times. The test of optical response characteristics shows (Figureure 6/ Table 2) : At A light intensity of 10mW/cm^2, the device's light responsivity (R) reaches 2.95 A/W, corresponding to an external quantum efficiency (EQE) of 564.54%, the specific detectivity (D*) increases to 2.63×1010 Jones, and the light-dark current ratio (Ilight/Idark) reaches 2.00.

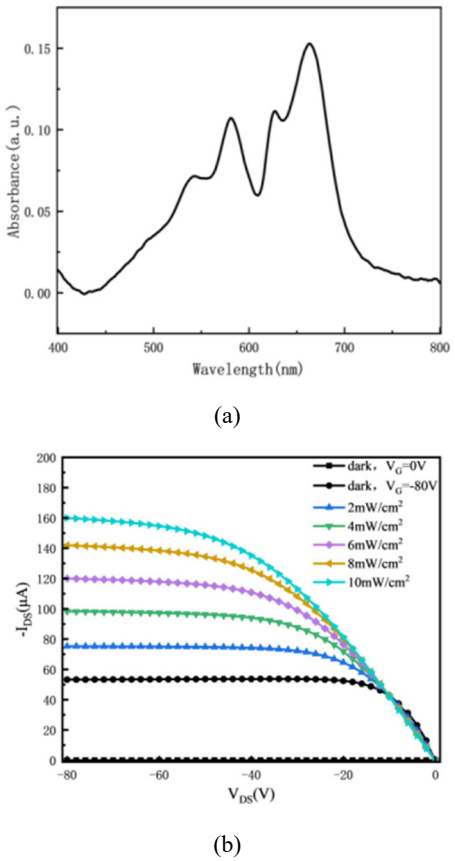


Figure. 6 (a)Absorption spectrum of pentacene thin films;(b)Output characteristics of the dual-modified device under varying light irradiation.

Table 2. Summary of device photosensitive characteristic parameters

Device	μ_{dark} $\times10^{-3}(cm^2/V\cdot s)$	μ_{light} $\times10^{-3}(cm^2/V\cdot s)$	R(A/W)	EQE(%)	D*(Jones)
(Unmodified)	2.19	3.22	0.69	131.63	1.52×10^{10}
(Modified)	6.36	16.5	2.95	564.54	2.63×10^{10}

Overall, the co-modification with OTS and PFBT significantly enhances the photoresponsivity, external quantum efficiency (EQE), specific detectivity (D*), and light/dark current ratio of the device. Combined with the improved pentacene film quality shown in Figureure 5, these results suggest that OTS passivates unsaturated dangling bonds on the SiO_2 surface. The inherent hydrophobicity of OTS further imparts hydrophobic characteristics to the SiO_2 surface. As a result, pentacene films deposited on OTS-modified SiO_2 exhibit denser and more uniform crystallites, reduced grain boundary gaps, and enhanced crystallinity. This structural optimization facilitates carrier transport while minimizing interfacial trap states and recombination centers, thereby reducing photogenerated carrier recombination and improving photoresponsivity[13].Meanwhile, PFBT modifies the Cu electrode through self-assembled monolayers (SAMs) formed by its volatile components. The fluorine-rich PFBT molecules on the Cu surface generate dipole moments oriented toward the metal substrate, increasing the electrode's work function to better align with the pentacene energy levels. the intrinsic work functions of pentacene and bare Cu are 5.0 eV and 4.58 eV[14], respectively, yielding a large work function mismatch. Post-modification, the Cu electrode's work function increases to 4.81 eV[15], achieving a 0.23 eV shift. The internal dipoles of PFBT-SAMs and their ordered

arrangement on the substrate enhance the Cu electrode's work function, reducing contact barriers and improving carrier injection efficiency.

4. Conclusion

This study employed Etched SiO_2 Layers and interface modification (OTS/PFBT) to optimize the SiO_2 dielectric layer and Cu electrodes in bottom-contact organic field-effect transistors (OFETs). The electrical and optical characteristics of the devices under dark and illuminated conditions were systematically investigated before and after etching/modification. OTS treatment enhanced the hydrophobicity of the SiO_2 surface, promoting the growth of denser, more uniform pentacene films with enlarged grains[13]. Subsequent PFBT modification elevated the work function of Cu electrodes (from 4.58 eV to 4.81 eV)[14], effectively reducing the contact barrier between Cu and pentacene ($\Delta\Phi$=0.23 eV) via dipole alignment within self-assembled monolayers (SAMs). This interfacial engineering improved carrier injection efficiency while suppressing trap-assisted recombination[15]. Post-optimization devices exhibited a maximum saturated current of 53.2 μA, field-effect mobility of 6.36×10^{-3} $cm^2/V\cdot s$, and threshold voltage of -16 V. Under 650 nm illumination at 10 mW/cm^2, the devices achieved a photoresponsivity of 2.95 A/W and external quantum efficiency (EQE) of 564.54%. These results demonstrate that tailored etching processes combined with interface modification significantly enhance OFET performance metrics, establishing a foundation for high-sensitivity OFET-based photodetectors. Future work focusing on etching parameter refinement and structural innovation could further advance device performance for optoelectronic applications.

Acknowledgments

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