# Design and Analysis of a Single-Switch Energy-Stacking DC–DC Converter for Renewable Energy Integration

Thai Anh Au Tran
Faculty of Electrical Engineering
University of Science and Technology, The University of Danang
Da Nang, Vietnam
ttaau@dut.udn.vn

* Corresponding author: ttaau@dut.udn.vn

Xuan Khanh Ho
University of Science and Technology, The University of Danang
Da Nang, Vietnam
hxkhanh.dut.ud@gmail.com

Hoai Khanh Ly Le
University of Science and Technology, The University of Danang
Da Nang, Vietnam
Kllh30052005@gmail.com

***Abstract*— A DC–DC power conversion topology based on a single controlled switch and high voltage elevation is developed, employing magnetic energy transfer and an integrated passive clamp to mitigate the voltage stress on the MOSFET. Operating at a duty cycle of 41.7%, the converter achieves an output–input voltage ratio of 16.67, stepping up from 24 V to 400 V. The proposed topology overcomes key limitations of conventional converters, including high losses at large duty cycles and excessive component counts in cascaded architectures. Comprehensive steady-state operation, voltage and current stress evaluation, power loss assessment, and passive component design are analytically investigated. Comparative evaluation with existing high step-up topologies and simulation validation are also presented. Simulation results under a 300 W output power condition demonstrate a peak efficiency of 95.44% and low output voltage ripple. The outcomes support the analytical framework and indicate the suitability of the proposed converter for real-world applications requiring stable high-voltage DC conversion from low-voltage sources.**

***Keywords—high step-up, DC-DC converter, coupled inductor, passive clamp, renewable energy, quadratic boost***

## I. Introduction

The global transition toward sustainable energy systems has substantially accelerated in response to the need to replace fossil fuel–based energy sources [1]. In response, many researchers have focused on improving the efficient utilization of these energy sources [2]–[3]. However, a common challenge is their low DC output voltage, commonly within the 20–40 V range. Meanwhile, applications encompassing electric transportation platforms and off-grid microgrid power systems, and auxiliary or backup power generation systems require a stable voltage of 380 V to 400 V for extended operation [4]–[9]. High-voltage DC generation has driven extensive research on boost DC–DC converters, whose ideal conversion ratio theoretically diverges as the duty cycle approaches unity. Practical parasitic effects significantly limit the attainable voltage boost to only several multiples of the input voltage [10]. Other solutions rely on multi-level voltage boosting schemes, capacitor-assisted switching networks, and staged converter configurations to achieve higher gain [11]–[13]. However, these approaches introduce new challenges, as achieving high gain requires connecting multiple stages, increasing design cost and overall circuit complexity. Recently, coupled inductor (CI) has emerged as a promising solution for high voltage gain (VG), enabling higher gain at lower duty cycles through the turn's ratio [14]–[15]. A key issue with this approach is leakage energy, which induces harmful voltage overshoots on the main MOSFET. Clamp circuits have been introduced to address this, effectively limiting the switch voltage [16]. Although achieving high gain with limited switch stress, these circuits often require many components, increasing complexity. Subsequent research has focused on reducing component count [17], but the use of multiple switches and two CIs means overall complexity remains a concern. Using multiple MOSFETs to achieve high gain has also been proposed [18]. However, this increases control and driver complexity, complicating practical design. Similar challenges are encountered in [19] and [20]; while the topology in [20] uses fewer components than [19], its VG is not yet optimal. Based on this analysis of advantages and limitations, the proposed converter (PC) is developed to accomplish the following goals:

- Enable effective energy recovery from leakage inductance
- High VG based on a CI.
- Using a single switch to simplify control.
- Limitation of MOSFET voltage stress (VS) via a diode–capacitor clamp structure.

- Reduced output voltage ripple.

The paper is organized into several sections. Section II presents the operating principles and a detailed analysis of the PC. Section III examines steady-state performance, including conversion ratio and device stress, and power dissipation, along with a comparative evaluation against existing topologies to highlight key advantages. Section IV provides simulation-based verification of the theoretical framework. Section V presents the final conclusions of this study by summarizing the main contributions and discussing practical implementation aspects.

## II. The PC And Analyses Operating

### *A. Topology of the PC*

The PC structure is presented in Figure 1, with the following component count: seven diodes ($D_1 \sim D_6$ and output diode $D_o$); six capacitors ($C_1 \sim C_5$ and output capacitor $C_o$); one inductor $L_1$; one CI with primary winding denoted as $N_p$ and secondary winding as $N_s$. The turns ratio is defined as $n = N_s/N_p$ , with the dot convention indicated in the figure. Leakage energy is modeled by the inductor $L_k$. A single main switch $S_1$, together with a passive clamp formed by $D_3$ and $C_3$, limits the VS across the main switch.

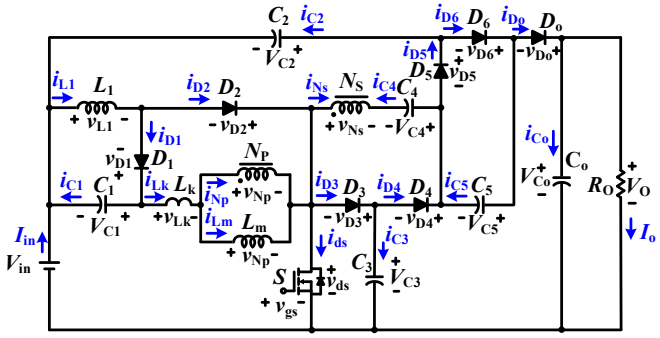


Figure. 1. The PC structure.

### *B. Operating Principles*

Fig. 2 depicts the Continuous Conduction Mode (CCM) waveforms, while the corresponding operational stages are presented in Fig. 3. For analytical convenience, the influence of $L_k$ and non-ideal resistances is neglected. Additionally, all capacitors are assumed to be sufficiently large to preserve a steady voltage across them during one switching cycle.

*Stage I* ($t_0 \le t \le t_1$) [Fig. 3(a)]: At $t = t_0$, When $v_{gs}$ is high, $S$ conducts. $D_1$, $D_3$, $D_5$ and $D_o$ are OFF, while the remaining diodes are ON. $C_4$ is charged by energy from $V_{in}$, $C_1$, and $L_k$ through $N_s$ of the CI, as well as from $C_3$. $L_1$ receives energy from $V_{in}$ via $D_2$ and $S_1$. $L_m$ receives energy from both $V_{in}$ and $C_1$. $C_5$ is powered by $V_{in}$ and $C_2$. $C_o$ supplies power to the output. This stage completes as $v_{gs1}$ goes low at $t_1$. The voltage relations follow Kirchhoff's voltage law (KVL):

$$v_{L1} = V_{in} \quad (1)$$
$$v_{Lm} = V_{C1} + V_{in} \quad (2)$$
$$v_{N_s} = V_{C4} + V_{C5} - V_{C2} - V_{in} \quad (3)$$
$$V_{C4} = v_{N_s} + V_{C3} \quad (4)$$

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*Stage II* ($t_1 \le t \le t_2$) [Fig. 3(b)]: At $t = t_1$, $v_{gs}$ is low. $D_1$, $D_3$, and $D_o$ conduct, while the other diodes are OFF. Capacitor $C_1$ is charged by $L_1$. Meanwhile, $V_{in}$, $L_1$, $L_m$, and $L_k$ charge $C_3$ through $D_3$. Due to leakage energy, $L_k$ helps charge $C_3$ and this stored energy is used to supply the load in the next switching cycle, achieving effective leakage energy recycling. A passive voltage clamp formed by $D_3$ and $C_3$ limits the voltage stress across the main switch, preventing damaging voltage spikes. The output capacitor $C_o$ is charged by energy from the CI, $L_k$, $V_{in}$, $L_1$, $C_4$, and $C_5$ via $D_1$ and $D_o$, resulting in a significantly boosted output voltage. This stage ends when capacitor $C_3$ is fully charged and $D_5$ begins to conduct at $t = t_2$. The following voltage equations are obtained:

$$v_{L1} = -V_{C1} \quad (5)$$
$$v_{Lm} = V_{in} - v_{L1} - V_{C3} \quad (6)$$
$$V_{C0} = V_{in} - v_{L1} - v_{Lm} - v_{N_s} + V_{C4} + V_{C5} \quad (7)$$

*Stage III* ($t_2 \le t \le t_3$) [Fig. 3(c)]: At $t = t_2$, $v_{gs}$ is still low. This stage is similar to Stage II, with the key difference that $D_5$ conducts and $C_2$ is powered by $L_1$, the CI, $L_k$, and $C_4$. This stage ends when $v_{gs}$ goes high again, completing the switching cycle at $t = t_3$. The voltage equations arise:

$$V_{C2} = -v_{L1} - v_{Lm} - v_{N_s} + V_{C4} \quad (8)$$

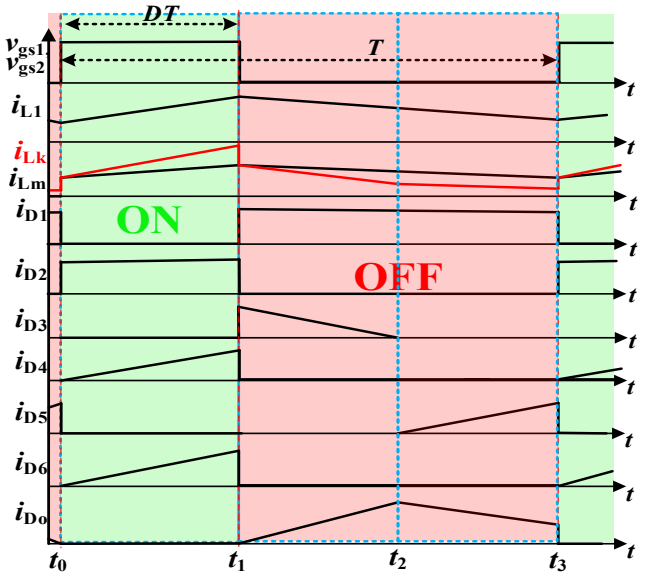
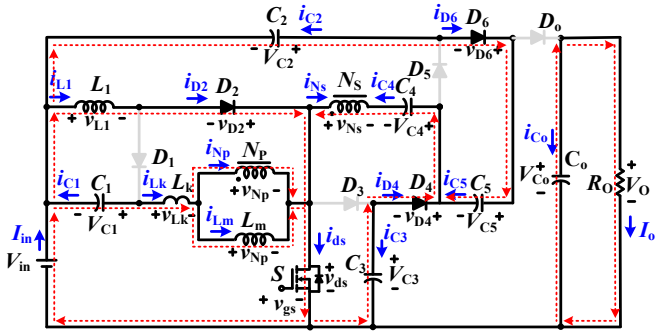
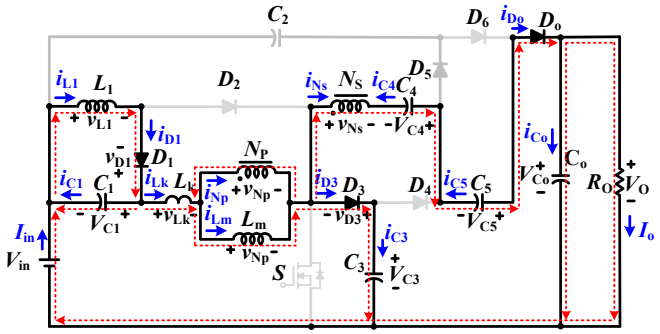


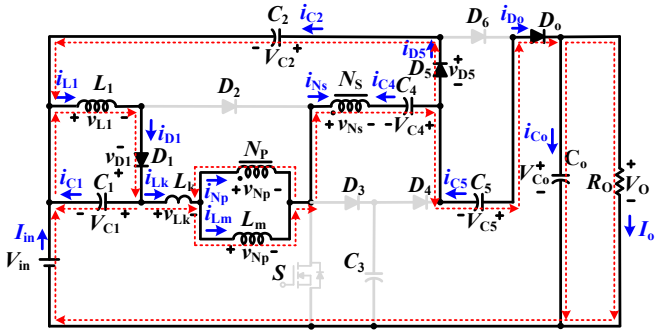

Figure. 2. The key waveforms under CCM.



(a) Mode I



(b) Mode II



(c) Mode III

Figure. 3. The key waveforms under CCM.

### C. *Steady state analysis of the PC*

Applying volt–second balance (AVB) on $L_1$ with (1) and (5) yields:

$$\frac{1}{T}\int_0^{DT} V_{\text{in}}dt + \frac{1}{T}\int_{DT}^{T}(-V_{\text{C1}})dt = 0 \tag{9}$$

Using (9), the voltage $C_1$ is:

$$DV_{\text{in}} + (1-D)(-V_{\text{C1}}) = 0 \rightarrow V_{\text{C1}} = \frac{DV_{\text{in}}}{1-D} \tag{10}$$

Using the AVB to $L_{\text{m}}$ and (2) & (6) yields:

$$\frac{1}{T}\int_0^{DT}(V_{\text{C1}} + V_{\text{in}})dt + \frac{1}{T}\int_{DT}^{T}(V_{\text{in}} - v_{\text{L1}} - V_{\text{C3}})dt = 0 \tag{11}$$

The voltage equation for $C_3$ is derived based on (11):

$$D(V_{\text{C1}} + V_{\text{in}}) + (1-D)(V_{\text{in}} + V_{\text{C1}} - V_{\text{C3}}) = 0$$
$$\rightarrow V_{\text{C3}} = \frac{V_{\text{in}}}{(1-D)^2} \tag{12}$$

Combining (4) and (12) gives the $C_4$ voltage:

$$V_{\text{C4}} = n\frac{V_{\text{in}}}{1-D} + \frac{V_{\text{in}}}{(1-D)^2} = \frac{(1+n-Dn)V_{\text{in}}}{(1-D)^2} \tag{13}$$

Based on Equation (8), together with the capacitor voltage expressions previously established in (10), (12), and (13), the voltage $C_2$ is:

$$V_{\text{C2}} = \frac{DV_{\text{in}}}{1-D} + (1+n)\frac{DV_{\text{in}}}{(1-D)^2} + \frac{(1+n-Dn)V_{\text{in}}}{(1-D)^2}$$
$$\rightarrow V_{\text{C2}} = \frac{(2D - D^2 + n + 1)V_{\text{in}}}{(1-D)^2} \tag{14}$$

Using Equation (3), the $C_5$ voltage is:

$$V_{\text{C5}} = V_{\text{in}} + n\frac{V_{\text{in}}}{1-D} + \frac{(2D - D^2 + nD)V_{\text{in}}}{(1-D)^2}$$
$$\rightarrow V_{\text{C5}} = \frac{(\text{n}+1)V_{\text{in}}}{(1-D)^2} \tag{15}$$

From (7), the $V_{\text{Co}}$ voltage is:

$$V_{\text{Co}} = V_{\text{in}} + \frac{(2D - D^2 + n + 1)V_{\text{in}}}{(1-D)^2} + \frac{(n+1)V_{\text{in}}}{(1-D)^2}$$
$$\rightarrow V_{\text{Co}} = \frac{(2n+3)V_{\text{in}}}{(1-D)^2} \tag{16}$$

The VG of the PC is formulated from (16):

$$G = \frac{V_{\text{o}}}{V_{\text{in}}} = \frac{(2n+3)}{(1-D)^2} \tag{17}$$

### D. *VS*

When $S$ and is OFF (Fig. 3(b)), $S$ becomes clamped in parallel with capacitor $C_3$ through diode $D_3$. Therefore, the VS on the two switches are:

$$v_{\text{ds}} = V_{\text{C3}} = \frac{V_{\text{in}}}{(1-D)^2} \tag{18}$$

The Diode voltage stresses:

$$v_{\text{D1}} = V_{\text{C1}} + V_{\text{in}} = \frac{V_{\text{in}}}{1-D} \tag{19}$$

$$v_{\text{D2}} = V_{\text{C3}} - V_{\text{C1}} - V_{\text{in}} - = \frac{DV_{\text{in}}}{(1-D)^2} \tag{20}$$

$$v_{\text{D3}} = V_{\text{C3}} = \frac{V_{\text{in}}}{(1-D)^2} \tag{21}$$

$$v_{\text{D4}} = V_{\text{C4}} - n(V_{\text{in}} - v_{\text{L1}} - V_{\text{C3}}) = \frac{(\text{n}+1)V_{\text{in}}}{(1-D)^2} \tag{22}$$

$$v_{\text{D5}} = V_{\text{C5}} = \frac{(\text{n}+1)V_{\text{in}}}{(1-D)^2} \tag{23}$$

$$v_{\text{D6}} = V_{\text{C5}} = \frac{(\text{n}+1)V_{\text{in}}}{(1-D)^2} \tag{24}$$

$$v_{\text{Do}} = V_{\text{Co}} - V_{\text{C3}} - V_{\text{C5}} = \frac{(\text{n}+1)V_{\text{in}}}{(1-D)^2} \tag{25}$$

### E. *Current stress.*

The average current for each device is derived from the operating states in Figure 3. A Full set of these expressions is given in Table I.

TABLE I. THE AVERAGE AND RMS CURRENT

| | | | |
|---|---|---|---|
| **Diodes** | | | |
| | | **Ave-current** | **RMS-current** |
| $D_1$ | | $\frac{(3+2n)I_o}{1-D}$ | $\frac{(3+2n)I_o}{(1-D)\sqrt{(1-D)}}$ |
| $D_2$ | | $\frac{(1-D)I_{in}-(3+2n)I_o}{1-D}$ | $\frac{(1-D)I_{in}-(3+2n)I_o}{(1-D)\sqrt{D}}$ |
| $D_3$ | | $I_o$ | $\frac{I_o}{\sqrt{1-D}}$ |
| $D_4$ | | $I_o$ | $\frac{I_o}{\sqrt{D}}$ |
| $D_5$ | | $I_o$ | $\frac{I_o}{\sqrt{1-D}}$ |
| $D_6$ | | $I_o$ | $\frac{I_o}{\sqrt{D}}$ |
| $D_o$ | | $I_o$ | $\frac{I_o}{\sqrt{1-D}}$ |
| **Capacitors** | | | |
| | | **Ave-current** | **RMS-current** |
| $C_1$ | | 0 | $\frac{(3D+2n)I_o}{(1-D)\sqrt{D(1-D)}}$ |
| $C_2$ | | 0 | $\frac{I_o}{\sqrt{D(1-D)}}$ |
| $C_3$ | | 0 | $\frac{I_o}{\sqrt{D(1-D)}}$ |
| $C_4$ | | 0 | $\frac{2I_o}{\sqrt{D(1-D)}}$ |
| $C_5$ | | 0 | $\frac{I_o}{\sqrt{D(1-D)}}$ |
| $C_o$ | | 0 | $\frac{I_o\sqrt{D}}{\sqrt{1-D}}$ |
| **Switches** | | | |
| | | **Ave-current** | **RMS-current** |
| $S$ | | $I_{in}-I_o$ | $\frac{I_{in}-I_o}{\sqrt{D}}$ |
| **Inductors** | | | |
| | | **Ave-current** | **RMS-current** |
| $L_1$ | | $I_{in}$ | $I_{in}$ |
| $CI$ | $L_m$ | $\frac{(3+2n)I_o}{1-D}$ | $\frac{(3+2n)I_o}{1-D}$ |
| | $N_s$ | 0 | $\frac{2I_o}{\sqrt{D(1-D)}}$ |

*F. Power loss.*

Under practical operating conditions, parasitic elements within MOSFETs, diodes, and passive components generate both conduction and switching losses, negatively impacting overall efficiency and system longevity. Hence, quantifying power dissipation in individual components is vital for optimizing device selection. The resulting loss analyzes are compiled in Tables I and II. Based on parameters derived from standard datasheets, the system attains maximum efficiency of 95.23% at a full load of 300 W: $r_{ds\_ON} = 3.8$ mΩ, $t_r = 15$ ns, $t_f = 17$ ns, $f_s = 50$ kHz, $R_{Load} = 533$ Ω, $V_{in} = 24$ V, $n = 1.5$, $V_{FO} = V_{F1} = V_{F2} = V_{F3} = V_{F4} = V_{F5} = V_{F6} = 0.45$ V, $r_{D1} = r_{D2} = r_{D3} = r_{D4} = 1$ mΩ, $r_{L1} = 10$ mΩ, $r_{N_p} = 5$ mΩ , $r_{N_s} = 7$ mΩ , $r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{C5} = 15$ mΩ, $r_{CO} = 5$ mΩ.

TABLE II. COMPONENT LOSS DISTRIBUTION

| Components | | Loss Formula | Power loss (W) |
|---|---|---|---|
| Diodes (55.1%) | $D_1$ | $r_{D1}.I^2_{D1\_RMS} + V_{F\_D1}.I_{D1\_ave}$ | 3.595 |
| | $D_2$ | $r_{D2}.I^2_{D2\_RMS} + V_{F\_D2}.I_{D2\_ave}$ | 2.603 |
| | $D_3$ | $r_{D3}.I^2_{D3\_RMS} + V_{F\_D3}.I_{D3\_ave}$ | 0.338 |
| | $D_4$ | $r_{D4}.I^2_{D4\_RMS} + V_{F\_D4}.I_{D4\_ave}$ | 0.339 |
| | $D_5$ | $r_{D5}.I^2_{D5\_RMS} + V_{F\_D5}.I_{D5\_ave}$ | 0.338 |
| | $D_6$ | $r_{D6}.I^2_{D6\_RMS} + V_{F\_D6}.I_{D6\_ave}$ | 0.339 |
| | $D_o$ | $r_{Do}.I^2_{Do\_RMS} + V_{F\_Do}.I_{Do\_ave}$ | 0.338 |
| Mosfets (15.1%) | $S$ | $r_{ds\_ON}.I^2_{ds\_RMS} + \frac{1}{2}v_{ds}.I_{S\_ave}(t_r + t_f)f$ | 2.163 |
| Capacitors (14.75%) | $C_1$ | $r_{C1}.I^2_{C1\_RMS}$ | 1.869 |
| | $C_2$ | $r_{C2}.I^2_{C2\_RMS}$ | 0.035 |
| | $C_3$ | $r_{C3}.I^2_{C3\_RMS}$ | 0.035 |
| | $C_4$ | $r_{C4}.I^2_{C4\_RMS}$ | 0.139 |
| | $C_5$ | $r_{C5}.I^2_{C5\_RMS}$ | 0.035 |
| | $C_o$ | $r_{Co}.I^2_{Co\_RMS}$ | 0.002 |
| Inductors (15.05%) | $L_1$ | $r_{L1}.I^2_{L1\_RMS}$ | 1.789 |
| | $L_m$ | $r_{Lm}.I^2_{Lm\_RMS}$ | 0.301 |
| | $N_S$ | $r_{N_s}.I^2_{Ns\_RMS}$ | 0.065 |
| Total loss | | | 14.323 |

*G. Inductor design.*

- To guarantee CCM condition and minimize current ripple, the inductor $L_1$ is sized so that half the peak-to-peak ripple current is at least the average current ($\Delta i_{L1}/2 \geq i_{L1\_ave}$).

$$L_1 \geq \frac{DTV_{in}}{2.I_{in}} \tag{26}$$

Where $\Delta i_{L1}$ denotes the current ripple across inductor $L_1$.

- The inductor $L_m$ is also designed using a similar condition, and its inductance value is obtained as follows:

$$L_1 \geq \frac{V_{in}DT}{2I_o(3+2n)} \tag{27}$$

*H. Capacitor design.*

Capacitors $C_1$ to $C_5$ are designed based on the triple VS, determined by the following formula:

$$C_1 = \frac{I_o(3D+2n)}{\Delta v_{C1}.f_s};\ C_2 = \frac{I_o}{\Delta v_{C2}.f_s};\ C_3 = \frac{I_o}{\Delta v_{C3}.f_s}$$
$$C_4 = \frac{I_o}{\Delta v_{C4}.f_s};\ C_5 = \frac{I_o}{\Delta v_{C5}.f_s} \tag{28}$$

$C_o$ is chosen to minimize output voltage fluctuation, and its capacitance is determined as follows:

$$C_o = \frac{V_oDT}{R_o\Delta v_{Co}} \tag{29}$$

## III. Comparison With Other Topologies

A comparative study with related topologies is performed to assess the advantages of the PC. For fairness, the designs in [17] and [19] are normalized to a fixed turns ratio of n = 1.5. The comparison encompasses the following aspects:

Total Component Count: The PC uses fewer components than [16], [18], and [19], providing a clear advantage in design simplicity.

VG: Against the topologies in Table III, the PC offers a higher VG, resulting in a wider and more flexible boost range designed for renewable energy platforms. The gain curves are compared in Fig 4.

VS on Main MOSFET: Comparison of VS on the MOSFET is shown in Fig 5. The structure features a relatively low VS that is independent of the duty cycle, facilitating low resistance devices

TABLE III. Comparison with published topologies

| Ref. | Number of components | | | | | G | Voltage stress of main switch ($/V_o$) | Power (W) | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|---|
| | S | D | C | CI | I | T | | | |
| [16] | 1 | 8 | 8 | 1 | 0 | 18 | $\frac{2+2n+D}{1-D}$ | $\frac{1}{2+2n+D}$ | 200 | 95.89 |
| [17] | 2 | 6 | 6 | 2 | 0 | 16 | $\frac{2n+4}{1-D}$ | $\frac{1}{2n+4}$ | 500 | 97.29 |
| [18] | 3 | 6 | 6 | 1 | 2 | 18 | $\frac{2+n+nD}{(1-D)^2}$ | $\frac{1-D}{2+n+nD}$ | 500 | 95.52 |
| [19] | 2 | 8 | 6 | 2 | 0 | 18 | $\frac{2+2n}{(1-D)^2}$ | $\frac{1}{2+2n}$ | 150 | 95 |
| [20] | 2 | 6 | 6 | 1 | 1 | 16 | $\frac{1+2n}{(1-D)^2}$ | $\frac{1}{1+2n}$ | 175 | 93 |
| PC | 1 | 7 | 6 | 1 | 1 | 16 | $\frac{3+2n}{(1-D)^2}$ | $\frac{1}{3+2n}$ | 300 | 95.44 |

**Note**: **S** = Switchs; **D** = Diodes; **C** = Capacitors; **CI** = Coupled inductor; **I** = Inductors; **T** = Total devices; **VG** = voltage gain.

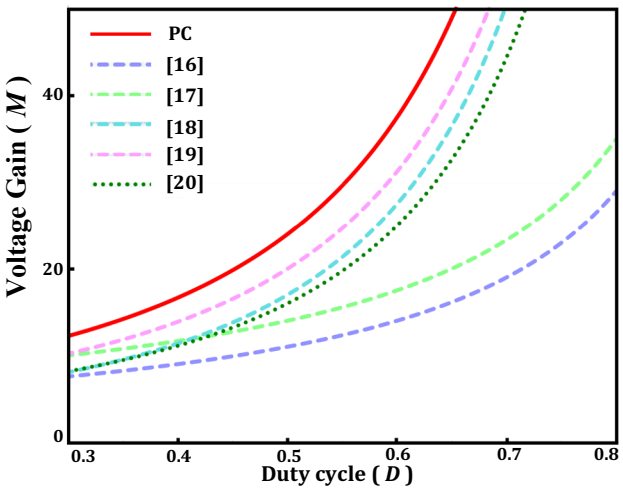



Figure. 4. The VG curves are compared in Table III.

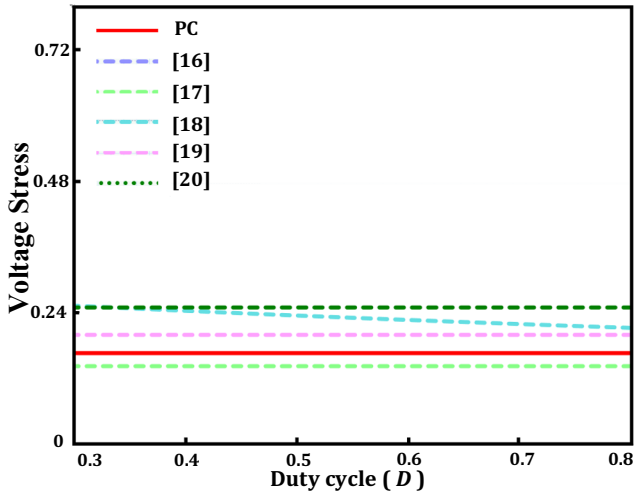



Figure. 5. The comparison curve of VS on the main switch is illustrated in Table III.

## IV. SIMULATION RESULSTS

The theoretical analysis is verified through simulations. The simulation parameters are summarized in Table IV, while Fig. 6 depicts the simulated circuit and Fig. 7 presents the resulting waveforms.

TABLE IV. Key parameters used in the simulation

| Device name | Value |
|---|---|
| $P_o$ | 300 W |
| $V_o$ | 400 V |
| $V_{in}$ | 24 V |
| $f$ | 50 kHz |
| $L_1$ | 100 μH |
| $L_m$ | 55 μH |
| $L_k$ | 1 μH |
| Turn ratio ($n = N_s/N_p$) | 1.5 |
| $C_1 \sim C_5$ | 63 μF |
| $C_o$ | 330 μF |

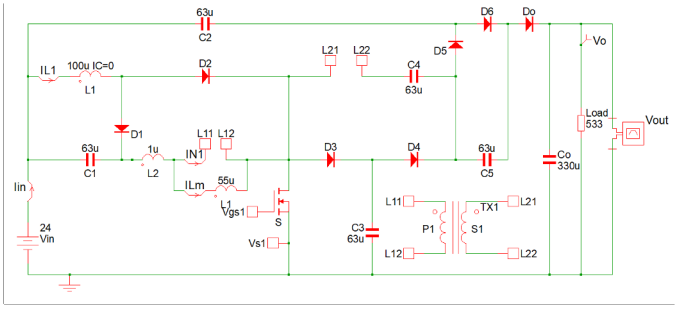
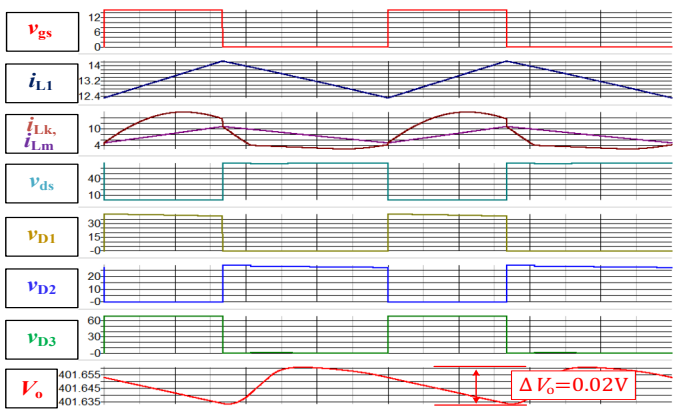
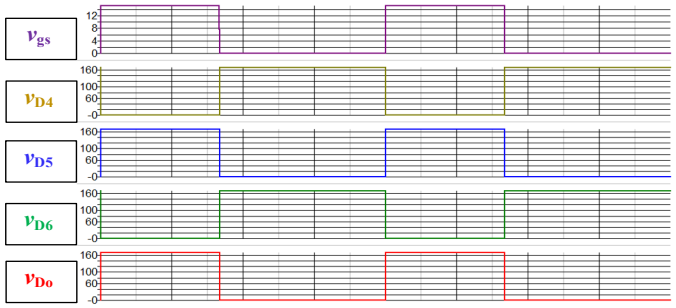



Figure. 6. Simulation schematic of the structure.




(a) $v_{gs}$, $v_{ds}$, $i_{L1}$, $i_{Lm}$ & $i_{Lk}$, $v_{D1} - v_{D3}$ and $V_o$.




(b) $v_{gs}$, $v_{D4} - v_{D6}$ and $v_{Do}$

Figure. 7. Simulation waveforms of the PC.

Fig. 7 shows that:

- Voltage Analysis: Under simulation conditions at a duty cycle of 41.7%, the switch VS ($v_{ds}$) is measured at 68 V for $V_O$ of 400 V. These results confirm the theoretical analysis, establishing a solid foundation for hardware implementation. The low VS across the switches supports low-resistance MOSFET utilization, thereby lowering switching losses and improving efficiency.
- Output Voltage Stability: The output capacitors $C_o$ effectively suppress output voltage ripple, achieving a simulated ripple voltage $\Delta V_o$ of just 0.02 V. This low ripple characteristic makes the PC tailored to applications demanding a stable voltage supply, such as renewable energy systems.

## V. CONCLUSION

A quadratic boost converter integrating a CI and single switches is presented. The design offers optimized component usage and high VG. Simulation outcomes corroborate the analytical results and demonstrate operational effectiveness. At 300 W, the PC shows 95.44 % efficiency and low switch VS, permitting low $r_{ds\_ON}$ MOSFETs. The output capacitor also minimize ripple, making it ideal for stable DC supply in renewable energy applications.

## ACKNOWLEDGMENT

## REFERENCES

[1] C. Li, H. Li, L. Cheng, X. Sun, N. Wang, and W. Li, “A novel non-isolated dual-input single-output high step-up DC/DC converter with coupled inductors,” IEEE Trans. Power Electron., vol. 38, no. 9, pp. 11556–11567, Sep. 2023.

[2] K. A. Nguyen, T. A. A. Tran, X. Khanh Ho and D. Thach Pham, "A Two-Switch Step-Up Topology With Coupled Inductor for High Voltage Conversion," IEEE Access, vol. 13, pp. 154326-154340, 2025.

[3] W. Chen, X. Wu, L. Yao, W. Jiang, and R. Hu, ‘‘A step-up resonant converter for grid-connected renewable energy sources,’’ IEEE Trans. Power Electron., vol. 30, no. 6, pp. 3017–3029, Jun. 2015.

[4] M. K. Singla, P. Nijhawan, and A. S. Oberoi, ‘‘Hydrogen fuel and fuel cell technology for cleaner future: A review,’’ Environ. Sci. Pollut. Res., vol. 28, no. 13, pp. 15607–15626, Apr. 2021.

[5] T. A. A. Tran, X. K. Ho, D. T. Pham, T. N. A. Le, and K. Ánh Nguyễn, “A Quadratic high-step-up DC–DC converter architecture for renewable-energy applications”, MCA, pp. 26–35, Feb. 2026.

[6] P. Mohseni, S. H. Hosseini, M. Sabahi, T. Jalilzadeh, and M. Maalandish, “A new high step-up multi-input multi-output DC–DC converter,” IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5197–5208, Jul. 2019.

[7] S. Hasanpour, Y. P. Siwakoti, A. Mostaan, and F. Blaabjerg, “New semiquadratic high step-up DC/DC converter for renewable energy applications,” IEEE Trans. Power Electron., vol. 36, pp. 433–446, 2021.

[8] H. Bi, P. Wang, and Y. Che, ‘‘A capacitor clamped H-type boost DC-DC converter with wide voltage-gain range for fuel cell vehicles,’’ IEEE Trans. Veh. Technol., vol. 68, no. 1, pp. 276–290, Jan. 2019

[9] G. Rajendran, R. Raute, and C. Caruana, ‘‘A comprehensive review of solar PV integration with smart-grids: Challenges, standards, and grid codes,’’Energies,vol.18,no.9,p.2221,Apr.2025, doi: 10.3390/en18092221

[10] J. Jiang, T. Zhang, and D. Chen, “Analysis, design and implementation of a differential power processing DMPPT with multiple buck–boost choppers for photovoltaic module,” *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10214–10223, Mar. 2021.

[11] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, “Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications,” IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[12] W. Li and X. He, “Review of nonisolated high-step-up DC–DC converters in photovoltaic grid-connected applications,” IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[13] M. K. Nguyen, T. D. Duong, and Y. C. Lim, “Switched-capacitor-based dual-switch high-boost DC–DC converter,” IEEE Trans. Power Electron., vol. 33, no. 5, pp. 4181–4189, May 2017.

[14] Z. Chen, Q. Zhou, and J. Xu, “Coupled-inductor boost integrated flyback converter with high-voltage gain and ripple-free input current,” IET Power Electron., vol. 8, no. 2, pp. 213–220, Feb. 2015.

[15] X. Fan, H. Sun, Z. Yuan, Z. Li, R. Shi, and N. Ghadimi, “High voltage gain DC–DC converter using coupled inductor and VM techniques,” IEEE Access, vol. 8, pp. 131975–131987, Jan. 2020.

[16] A. Sepahvandi, B. Rezaeealam, and M. Mikhak-Beyranvand, “A single switch high step-up DC–DC converter derived from coupled inductor and switched capacitor for a photovoltaic system,” Sci. Rep., vol. 14, no. 1, art. no. 28042, Nov. 2024.

[17] S. W. Seo, J. H. Ryu, Y. Kim, and J. B. Lee, “Ultra-high step-up interleaved converter with low voltage stress*,” IEEE Access,* vol. 9, pp. 37167–37178, Mar. 2021.

[18] I. K. Denholm, W. Hassan, M. Negnevitsky, and D. D.-C. Lu, “Optimized interleaved ultra-high gain DC-DC power converter with low ripple input current and voltage stress for fuel cell systems,” IEEE Access, vol. 12, pp. 121052–121063, Aug. 2024.

[19] Samuel, V.J., Keerthi, G. and Mahalingam, P. (2020), Coupled inductor-based DC–DC converter with high voltage conversion ratio and smooth input current. IET Power Electronics, 13: 733-743. https://doi.org/10.1049/iet-pel.2019.0933.

[20] P. Upadhyay, R. Kumar, and S. Sathyan, “Coupled-inductor-based high-gain converter utilising magnetising inductance to achieve soft-switching with low voltage stress on devices,” IET Power Electron., vol. 13, no. 3, pp. 576–591, Mar. 2020